A High Performance CMOS Bandgap Voltage Reference With Offset Compensation Technique

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Abstract — A high precision CMOS band-gap voltage reference which takes the advantage of low power supply voltage and offset compensation is presented. In this method, the proposed two feedback loops in the opamps will optimize the $\Delta V_{BE}$ and hence the factor of offset can be minimized. The post layout simulation results shows that, the circuit achieves a much low temperature coefficient of $9ppm/\text{oC}$ over a temperature range of $-50 \text{C}$ to $+95 \text{C}$ with $1.2 \text{V}$ output reference voltage and a high PSRR over a broad frequency range. The PSRR is $-94\text{dB}$ up to 10KHz and remains at $-72\text{dB}$ at 3MHz. The area of the layout is $0.22 \times 0.155 \text{mm}^2$ with $0.18\text{um}$ CMOS process.

Keywords — Band-gap Voltage Reference; Low-Supply Voltage; PSRR; CMOS.

I. INTRODUCTION

Voltage reference circuitry is very important block in many applications such as RF circuits[1], power converters, high precision comparators, A/D and D/A converters and other communications systems which need high-accuracy reference voltage to provide high-resolution and high speed data conversions in low supply-voltage conditions. The reference voltage accuracy determines the maximum achievable performance of all Integrated Circuit systems. In this field, the research is focused on the PSRR enhancement[2,3], low voltage and low power dissipation technique[4,5]. Design of Band-gap reference voltage circuitry is compatible with CMOS process. In CMOS process, only parasitic bipolar transistors are available and amplifiers based on CMOS transistors have significantly large input voltage offsets[4]. This paper presents a method with reduced effect of opamp voltage offsets in producing a reference voltage in a low power supply environment.

II. CMOS BAND-GAP VOLTAGE REFERENCE

Band-gap voltage reference circuit is based on the principle of adding two voltages having equal and opposite TC(temperature coefficient) of 9ppm/oC over a temperature range of -50 C to +95 C with 1.2 V output reference voltage and a high PSRR over a broad frequency range. The PSRR is -94dB up to 10KHz and remains at -72dB at 3MHz. The area of the layout is $0.22 \times 0.155 \text{mm}^2$ with $0.18\text{um}$ CMOS process.

Where $V_1$ is thermal voltage and equal of $kT/q$ where $k$ is Boltzman constant, $T$ is Kelvin temperature, and $q$ is electron charge. Thus the output voltage with offset of the band-gap voltage reference $V_{REF}$ can be expressed as:

$$V_{REF} = V_{BE2} + (1 + \frac{R_2}{R_3})(V_1 \ln n + V_{OS})$$

Where $V_{BE2}$ which has a negative TC of -2.4mV/C is the base-emitter voltage of Q2, $V_{OS}$ is the offset voltage of op-amp. From equation (2) by choosing an appropriate factor $n$ and ratio of $R_2$ and $R_3$, the temperature coefficient of $V_{REF}$ could be compensated by opposite terms.

![Fig 1. Typical Band-gap voltage reference with offset uncompensated](image)

However, in order to balance the voltage with positive TC, $\Delta V_{BE}$ needs to be amplified by a factor. This amplification of the $\Delta V_{BE}$ has the effect of introducing offset voltages and as a result the reference voltage precision may be affected, especially in CMOS process[6].

A conventional method to reduce the effect of offset is setting the ratio of collector current densities of Q1 and Q2 in m and stacking another two bipolar transistors above Q1 and Q2 respectively[7]. Thus the band-gap reference $V_{REF}$ considering offset of op-amp can be expressed as...
\[ V_{\text{REF}} = 2V_{\text{BE}} + (1 + \frac{R_2}{R_1})[2V_T \ln(mn) + V_{\text{OS}}] \quad (3) \]

The effect of offset can be reduced as factor 1+(R2/R1) has been degraded. However, the problem is the output of \( V_{\text{REF}} \) is about 1.2V, it is difficult to produce such a voltage in low supply voltage environment.

III. PROPOSED CMOS BAND-GAP VOLTAGE REFERENCE

Considering equation (2) if the factor of \( V_{1 \ln n} \) is maximized meanwhile the factor of \( V_{\text{OS}} \) could be minimized, the output \( V_{\text{REF}} \) with least effect of offset will be acquired. The band-gap voltage reference circuit designed in this paper provides a positive TC voltage and a negative TC voltage by two feedback loop respectively, and requires different expressions of factors of \( V_{1 \ln n} \) and \( V_{\text{OS}} \).

Fig 2 shows the schematic of the low offset band-gap reference, there is startup circuit in this schematic. The circuit comprises a positive TC voltage generating cell and a negative TC voltage generating cell. The positive TC voltage generating cell is composed of stacked substrate bipolar transistors Q1, Q2, Q3 and Q4, impedances R1, R2, R3 and R4, a low noise op-amp A1 and another bipolar transistor Q5. In this cell A1, impedance R2 and bipolar transistor Q5 comprise a feedback loop to force the inverting and non-inverting inputs of A1 equal. The negative TC voltage comprise another feedback loop composed of op-amp A2, impedance R4 and a PMOS transistor M1 of the current mirror circuit. This feedback loop force the non-inverting input to be \( V_{\text{BE}} \), and the output resistor R4 and resistor R3 co-operate to set the closed gain of the op-amp A2.

As the stacked bipolar transistors Q1, Q2 and Q3, Q4 have different emitter areas and work in different collector currents, a positive TC voltage \( 2 \Delta V_{\text{BE}} \) is provided, the voltage across resistor R1 produces a current \( I_{\text{R1}} \).

\[ I_{\text{R1}} = 2 \Delta V_{\text{BE}} / R_1 \quad (4) \]

Under the situation of considering offset of op-amp the voltage of output of A1 expressed as:

\[ V_{\text{outA1}} = 2 V_{\text{BE}} + V_{\text{OS}} + ((2(\Delta V_{\text{BE}} + V_{\text{OS}})/R_1) * R_2) - V_{\text{BE}} \quad (5) \]

The inverting input voltage of op-amp A2 is expressed as:

\[ V_{\text{inA2}} = V_{\text{BE}} + V_{\text{OS}} \quad (6) \]

So the voltage between two ends of R3 is

\[ V_{R3} = ((2(\Delta V_{\text{BE}} + 2\Delta V_{\text{BE}} + V_{\text{OS}})/R_1) * R_2 \quad (7) \]

It is obvious that the offsets of op-amp A1 and A2 in equation (5) and (6) counteract. The reference voltage with offset is expressed as

\[ V_{\text{REF}} = V_{\text{BE}} + [2*(R_4/R_3)(1+(R_2/R_1))*\Delta V_{\text{BE}} + ((R_3R_4/R_1)+1)*V_{\text{OS}} \quad (8) \]

When setting the ratio of \( R_2/R_1 \) is 1, the ratio of \( R_4/R_3 \) is \( K \), the maximal factor of \( \Delta V_{\text{BE}} \) and minimal factor of \( V_{\text{OS}} \) are acquired. The reference voltage with offset is expressed as

\[ V_{\text{REF}} = V_{\text{BE}} + 4*K\Delta V_{\text{BE}} + (K+1) V_{\text{OS}} \quad (9) \]

Compared with equation (3), in equation (9) the factor of \( K \) could be a smaller value, and the effect of offset of op-amp has been reduced significantly. Additionally the band-gap voltage reference designed in this paper could be operated in a relative low supply voltage environment. The op-amp is a two-stage folded cascade differential op-amp with cascade PMOS loads and a push-pull stage is illustrated in Fig 3. This architecture is developed to improve the input common-mode voltage, gain, bandwidth, driving capability and PSRR of the typical two stage amplifier. On the stability consideration, the output stage is introduced the compensation miller capacitor \( C_1 \) and resistor \( R_8 \) to improve the phase margin.

![Fig 2. Proposed CMOS Band-gap voltage reference](image1)

![Fig 3. The op-amp circuit](image2)
IV. CADENCE SPECTRE POST LAYOUT SIMULATION RESULTS

In band-gap voltage reference, mismatches of resistors and bipolar transistors may seriously affect its performances. But it can be reduced or eliminated by an appropriate layout design to a great extent. In order to acquire accurate ratio of two resistors, a group of parallel sub-resistors with identical geometries are used, and the two resistors are arranged in the form of fork. In the layout of bipolar transistors, Q3, Q4 are composed of 8 blocks while Q1, Q2 are one. Meanwhile common-centroid layout is applied to achieve good matching[8]. Fig 4. shows the layout of the whole band-gap reference circuit. The area of layout is 0.22 x 0.155 mm$^2$ with a 0.18um CMOS process.

The post-simulations based on 0.18um CMOS process have been carried out. Table 1 gives the op-amp SPECTRE post-simulation results. Fig 2 shows the post-simulation result of output voltage of band-gap voltage reference versus temperature characteristics over the range form -50°C to 95°C, it can be seen that the peak-to-peak variation is just 1.55mV, the TC is 9ppm/C. Fig 6 shows the plot of supply rejection versus frequency. The power supply rejection ratio (PSRR) is -94dB up to 10 KHz. Table 2 summarizes the performances of the band-gap reference circuit.

**TABLE 1**

<table>
<thead>
<tr>
<th>PERFORMANCE OF OPAMP</th>
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<tbody>
<tr>
<td>Open-loop gain</td>
<td>94dB</td>
</tr>
<tr>
<td>Bandwidth at 0dB</td>
<td>14.4MHz</td>
</tr>
<tr>
<td>Phase margin</td>
<td>64.2°</td>
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<tr>
<td>Slew rate</td>
<td>36V/μs</td>
</tr>
<tr>
<td>PSRR at 10Hz</td>
<td>-84dB</td>
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<tr>
<td>PSRR at 1KHz</td>
<td>-67dB</td>
</tr>
<tr>
<td>PSRR at 1KHz</td>
<td>-14dB</td>
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</table>
TABLE 2

<table>
<thead>
<tr>
<th>Performance of Band-Gap Reference</th>
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<tbody>
<tr>
<td>Supply Voltage: 2.5V</td>
</tr>
<tr>
<td>Power Dissipation: 480u</td>
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<tr>
<td>Area: 0.22 x 0.155 mm²</td>
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<tr>
<td>TC: 9ppm/°C</td>
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<tr>
<td>PSRR at 3KHz: -94dB</td>
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V. Conclusions

A circuit, layout design and post-simulation results of a low offset band-gap voltage reference are proposed in this paper. Two feedback loops are introduced in the band-gap voltage reference circuit to increase the accuracy by reducing the effect of offsets of op-amps. The post-simulation results show that TC of the band-gap voltage reference is 9ppm/°C over the range from -50°C to 95°C. PSRR of the circuit is -90dB, the circuit produces a 1.2V reference voltage. The band-gap voltage reference is suitable to use in low voltage and high accuracy applications. This design has been used used as a current and voltage bias in a phase locked loop design and verified for its accuracy.

REFERENCES