Cascadable adiabatic logic circuits for low-power applications

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Abstract: There have been several strategies proposed to realise adiabatic circuits. Most of them require a clock signal and also its complement form. In this investigation, the authors we propose a family of adiabatic circuits, which consist of two branches and which enable control of charging and discharging of the capacitive load only by the input signal, work with single time varying supply and with no need of complementary inputs. A mathematical expression has been developed to explain the energy dissipation in our adiabatic inverter circuit. Measurements of energy drawn, recovered and dissipated have been carried out through simulation and, they are the same as obtained from the theoretical expression. In the proposed circuit, the input and output logic levels are approximately the same and can be used for building cascaded logic circuits. The energy saving in this family is to the tune of 50% compared with CMOS circuits constructed with similar circuit parameters, up to 250 MHz. The authors have described the proposed inverter, NAND gates, NOR gates, adder circuits and JK flip-flop along with their simulation results.

1 Introduction

In the literature, several adiabatic or energy recovery logic architectures have been proposed [1–5]. They have achieved significant power saving compared with conventional CMOS circuits. The outputs of these circuits are valid only during a particular phase of the power clock cycle. Hence, multiple-phase clocking is required to drive a chain of cascaded adiabatic logic circuits. The need for a multiple-phase power clock not only increases the power dissipation of the clocking network, but also results in extra complexity of both the logic and the required power clock generation. The 2N-2P and the 2N-2N2P circuits proposed by Kramer et al. [1], and the efficient charge recovery logic circuit proposed by Moon and Jeong [2] require four-phase clocking. The problem of floating point node in a pass-transistor adiabatic logic (PAL) inverter has been rectified in the PAL-2N circuit proposed by Liu and Lau [3], by using two minimised pull-down NMOS transistors. Although a single-phase clocking scheme is used in the design proposed by Maksimovic et al. [4], the extra demands of complementary control clock signals need to be met. Furthermore, the common feature of the above proposed circuits is that the input and output signals in a circuit do not appear in the same clock phase.

Younis and Knight [5] have proposed adiabatic logic families with less dissipation but each gate requires 16 times the number of devices compared with conventional logic. Dickinson and Denker [6] have used a diode-based dynamic logic to form the adiabatic dynamic logic (ADL) circuits. Reduction in power consumption has been achieved by pumping the energy stored in the load capacitor during the transition of output from logic ‘1’ to logic ‘0’. The drawbacks are that the gates are dynamic and a four-phase clocking is needed for cascading the gates. Further, the load capacitor is charged irrespective of the inputs and, hence, it has limited cascadability and sometimes it also produces unwanted outputs. Sathe et al. [7] proposed energy – efficient GHz-class charge – recovery logic, which needs the usage of additional power clocks and transistors to effect the boost operation.
Antonio and Saletti [8] proposed a positive feedback adiabatic logic gate, but this requires four-phase power clock and requires the input in its complement form also. Further, the capacitor is charged to logic ‘1’ before the evaluation phase and the output looks like a delayed version of the input. Shun, et al. [9] proposed quasi-static energy recovery logic with single power clock supply. In this logic, FET’s are connected as diodes (gate tied to one end of the channel) with the penalty that the effective forward drop across these devices is quite high (typically threshold voltage). Further, when the supply frequency is high, the power clock is coupled to the output of the gate because of the capacitance effect, causing unwanted charging and discharging of the output capacitance inducing a great deal of noise. Kim et al. [10] proposed true single-phase energy-recovering logic for low-power, high-speed VLSI, but this needs the input in its complement form also and the charge/discharge of output needed before the evaluation phase. NAKATA S [11] proposed ‘Adiabatic charging reversible logic using a switched capacitor regenerator’. This is based on the use of a capacitor regenerator and a binary decision diagram. The approach is based on switched capacitor circuits and the choice of the switching frequency is much higher than the frequencies to be processed.

We have proposed a glitch-free and cascadable adiabatic logic (GFCAL) family of adiabatic circuits, which can be easily cascaded without any glitch and can be operated by a single power source, and also do not need multi-phase clocks. In this paper, we describe the GFCAL inverter, NAND gates, NOR gates, adder circuits and JK flip-flop along with their simulation results. All these circuits have been found to consume power about 50% of that consumed by conventional CMOS circuits constructed with similar parameters.

2 GFCAL inverter

The structure of an adiabatic inverter proposed by us is shown in Fig. 1. This circuit consists of one P-channel MOSFET and a diode in parallel with one N-channel MOSFET and a diode, which in turn are connected in series with the load capacitance C as shown in Fig. 1. The supply voltage $V_{DD}$ is a slowly varying triangular voltage as shown in Fig. 2a. The P-channel MOSFET ($T_1$) and diode ($D_1$) provide a charging path, and the N-channel MOSFET ($T_2$) and diode ($D_2$) provide a discharging path for the load current.

2.1 Operation of the circuit

When the input is ‘0’ (logic ‘0’), $T_1$ is on and $T_2$ is off. Path $T_1, D_1$ allows the current flow from the supply and the capacitor becomes charged close to the peak value of $V_{DD}$, producing logic ‘1’. The diode $D_1$ does not allow discharge into the supply when $V_{DD}$ is less than the output voltage.

When the input is logic ‘1’, $T_2$ is on and $T_1$ is off. The path $D_2, T_2$ starts conducting. The diode, $D_2$ prevents charging of the capacitor since it is reverse biased when $V_{DD} > V_C$ and allows only discharging of the capacitor or pumping of energy back into the supply when $V_{DD} < V_C$. Thus, the capacitor voltage is brought down to a low value when the input is high irrespective of the previous output. Hence, the output is the complement of the input. Further, it is clear that the output voltage level is almost independent of the time at which the input voltage is applied with respect to the supply voltage as long as it is applied at a time before $V_{DD}$ reaches the peak value.

2.1.1 Estimation of energy dissipation in the inverter: The energy dissipated in the proposed inverter is calculated for a triangular supply voltage using the approximate expression derived by the authors.
1. Energy dissipation in the inverter during charging

When the P-channel MOSFET is on, and as \( V_{DD} \) increases from 0 to \( V_0 \), the load capacitor is charged through the diode in the charging path.

Consider the supply voltage \( V_{DD} \) as shown in Fig. 2a. The voltage reaches a peak value \( V_0 \) in a time period \( T \) and its value \( V_{DD}(t) \) at any time ‘\( t \)’ is

\[
V_{DD}(t) = \frac{V_0}{T} t, \quad \text{When } 0 \leq t \leq T
\]

\[
= V_0 \left[ 1 - \frac{(t - T)}{T} \right], \quad \text{When } T \leq t \leq 2T
\]

The voltage \( V_{DD}(t) \) reaches a value \( V_B \) in a period \( T_{th} \), when the diode starts conducting. Let \( R_{th} \) be the total resistance in the charging path.

The voltage \( V_C \) across the load capacitor ‘\( C \)’ for \( t > T_{th} \), is given by

\[
\frac{V_0}{T} t = V_B + R_{th} \frac{dV_C}{dt} + V_C
\]

Solving the above equation and assuming that \( T_{th} > CR_{th} \)

Energy \( E_{Ch} \) dissipated over the period \( 0 - T \) in the diode and the transistor can be shown to be

\[
E_{Ch} \approx V_0 C \left( R_{th} C \frac{V_0}{T} + V_B \right) \left( 1 - \frac{V_B}{V_0} \right)
\]

2. Energy dissipation in the inverter during discharging

When the N-channel MOSFET is on, and P-channel MOSFET is off, charging of the capacitor is prevented and the load capacitor discharges through the diode in the discharge path till \( t_1 \), that is, till \( V_C \) is higher than the supply by at least \( V_B \), during the period when \( V_{DD} \) increases from 0 to \( V_0 \). The capacitor then stops discharging at \( t_1 \) and again continues discharging from \( 2T-t_1 \) until \( V_C = V_B \). Let \( R_{dis} \) be the total resistance in the discharging path. Assuming \( CR_{dis} < t_1 \), the energy \( E_{dc} \) dissipated during discharging is the sum of energy dissipated during 0 to \( t_1 \) and \( 2T-t_1 \) to 2T which can be shown to be

\[
E_{dc} = t_1 \left( \frac{2V_0^2}{T^2} C^2 R_{dis} \right) - 2C \frac{V_0}{T} BCR_{dis} + V_B BC + \frac{B^2}{2} C
\]

where

\[
B = V_0 - V_B + R_{dis} \frac{V_0}{T}
\]

The total energy \( E_{dc} \), dissipated during one cycle of charging and discharging is given by

\[
E_D = E_{ch} + E_{dc} = V_0 C \left( R_{ch} C \frac{V_0}{T} + V_B \right) \left( 1 - \frac{V_B}{V_0} \right) + t_1 \left( \frac{2V_0^2}{T^2} C^2 R_{dis} \right) - 2C \frac{V_0}{T} BCR_{dis} + V_B BC + \frac{B^2}{2} C
\]

where, \( t_1 \) is given by

\[
t_1 = R_{dis} C \ln \left( \frac{V_C - V_B + (V_B R_{dis} C/T)}{V_0 R_{dis} C/T} \right)
\]

From (7), which is the theoretical expression for energy dissipation during charging and then discharging, it is clear that the energy dissipated decreases as \( T \) increases. Also, \( T \) indicates the rate at which the supply voltage varies and, hence, the energy dissipated decreases with slowly varying the supply voltages. Also, it indicates that the power dissipation generally changes with parameters like \( V_0 \), the value of the capacitance, the equivalent series resistance because of the diode and the MOSFET.

3 Simulation of inverter

The circuit of the inverter shown in Fig. 1 is simulated using VIRTUOSO SPECTRE circuit simulator of cadence EDA tools. The models used for this simulation are BSIM3V3 model parameters. The energy dissipated is calculated by subtracting the energy pumped back from the energy drawn. The theoretical and simulated values of energy dissipation for the adiabatic inverter are shown in Table 1 for the input data of ‘01’, that is, for one cycle of charging and discharging with the following circuit parameters. The length and the width of the transistor are 180 nm and 720 nm, respectively the value of load capacitance is 30 fF; the supply waveform is triangular; and the supply frequency is 25 MHZ. The input signal is a square wave with a frequency of 25 MHZ. The peak supply voltage is fixed at 1.8 V, which is enough to drive the transistors with reasonable logic values. The input logic ‘0’ value is 0.45 V and input logic ‘1’ value is 1.4 V. Along with the energy values, the output logic values have been found to be 0.45 and 1.4 V corresponding to logic ‘0’ and logic ‘1’.

<table>
<thead>
<tr>
<th>Name of the circuit</th>
<th>Energy dissipated, J</th>
<th>Simulation results</th>
<th>Theoretical value</th>
</tr>
</thead>
<tbody>
<tr>
<td>adiabatic inverter</td>
<td>4.04 × 10^{-14}</td>
<td>4.38 × 10^{-14}</td>
<td></td>
</tr>
<tr>
<td>CMOS inverter</td>
<td>9.12 × 10^{-14}</td>
<td>9.72 × 10^{-14}</td>
<td></td>
</tr>
</tbody>
</table>
respectively. From the Table 1, it is observed that for the adiabatic inverter, the simulated value of energy dissipation is comparable with the theoretical value obtained from (7).

With a view to comparing this energy dissipation with that of the CMOS inverter, the circuit of the CMOS inverter is simulated. The supply voltage for this circuit is 1.8 V, which is constant. The load capacitance, width and length of the transistors, and input data are the same as those of the adiabatic inverter. The energy dissipated as measured is given in Table 1. The calculated energy dissipated (\(CV^2\)) in the CMOS inverter for one cycle of charging and discharging is also given in Table 1 for the purpose of comparison. It may be seen that the measured energy dissipation is approximately the same as the calculated energy dissipation. From Table 1, for both the cases, it is clear that in our adiabatic inverter, the energy dissipation is only about 50% of that in the CMOS inverter.

### 3.1 Cascadability

From the model parameters used for simulation, the threshold voltage is 0.6 V for the N-channel MOSFET and −0.5 V for the P-channel MOSFET. Since the output value corresponding to logic ‘1’ in the simulated results is 1.4 V, which is higher than the threshold voltage, it can easily drive the following stages. Since the logic ‘0’ value is 0.45 V and peak value of supply voltage is 1.8 V, the peak value of voltage between gate and source \((V_{GS})\) of the p-channel MOSFET is

\[
V_{GS} = 0.45 - 1.8 = -1.35 V
\]

Hence, the output level corresponding to logic ‘0’ in the proposed inverter can drive the following stages. Further, it may be seen that, when the input is logic ‘1’, the output does not go through charging of the capacitor. This feature enables this circuit to be used to drive the circuits, which follow without malfunctioning. These aspects have been verified by connecting two, three and four inverters in tandem. Further, it may be noted that a single power supply for all the inverters is used.

### 3.2 Effect of variation of frequency

This simulation is carried out by Varying the input frequency and supply frequency simultaneously (keeping the input and supply frequencies equal) from 2.5 to 250 MHZ with all other circuit parameters remaining the same. The Variation of energy dissipated during one cycle of charging and discharging with the frequency of supply is given in Fig. 3 which indicates that the energy dissipated decreases marginally with increase in frequency. This is because the output logic levels up to frequencies of 25 MHZ are 1.4 V corresponding to logic ‘1’ and 0.45 V corresponding to logic ‘0’. At frequencies higher than 25 MHZ, it is found that the energy dissipated decreases gradually and the logic Values \(V_{GS}\) vary from 1.4 to 1.35 V for logic ‘1’ and 0.45 to 0.47 V for logic ‘0’ at 250 MHZ. At frequencies higher than 250 MHZ, the difference between logic ‘1’ and logic ‘0’ becomes small and at 2.50 GHZ, the logic ‘1’ tends to a Value of 0.8 V and logic ‘0’–0.6 V. This is because the time period of the supply waveform is small compared with the time constant of charging and discharging, and the capacitor is unable to charge and discharge to the required levels. Thus, the circuit with the above-mentioned parameters can work reasonably well up to 250 MHZ. One can increase the frequency of operation by increasing the width of the transistors, which results in a decrease of the charging and discharging time constants. It has been found that the frequency of operation can go up to an input frequency of 1 GHZ and a supply frequency of 2 GHZ when the width of the transistor is increased to 10 \(\mu\m\), keeping all other parameters of the circuit the same. However, it may be realised that realising transistors with a large \(W/L\) ratio results in higher power dissipation in both the CMOS and GFCAL circuits.

The variation of energy dissipation and the rise and fall times during one cycle of charging and discharging, with the varying supply frequency and the constant input data frequency of 5 MHZ are shown in Table 2. From these results, it is observed that the rise and fall times are reduced at higher values of the supply frequency but with a marginal increase of energy dissipation.

### 3.3 Effect of supply voltage waveforms

This experiment aims at describing the energy dissipated during 12 cycles of charging and discharging when the supply voltage is a sine, clamped to a zero reference level and a trapezium waveform with the other circuit parameters as indicated in Section 3. The input and the supply frequencies are synchronised. The energy dissipated when different supply waveforms are applied is indicated in Table 3. It may be seen from this table that the energy dissipation in the case of a trapezium waveform is more
than that in the case of a triangular waveform. It may be attributed to the fact that the capacitor is allowed to charge to a higher value of voltage corresponding to logic ‘1’ since the duration of the peak value of supply voltage is longer compared with that of the triangular waveform. In the case of the sine wave, the energy dissipation is more than that in the above cases, and this may be attributed to the fast voltage rise near the zero crossing. Thus, this measurement indicates that the triangular supply waveform is suitable for less energy dissipation.

4 GFCAL NOR and NAND gates

The structure of an adiabatic NOR gate proposed by us is shown in Fig. 4b. This circuit consists of two branches in parallel. The first branch consists of two P-channel MOSFETS (T1, T2) and a diode (D1) in series. The second branch consists of two N-channel MOSFETS (T3, T4) in parallel, connected in series with a diode (D2). The two parallel branches are connected in series with the load capacitance C as shown in Fig. 4b. The structure of an adiabatic NAND gate is shown in Fig. 4a. This circuit consists of two branches in parallel. The first branch consists of two P-channel MOSFETS (T5, T6) in parallel and a diode (D3) in series. The second branch consists of two N-channel MOSFETS (T7, T8) and a diode (D4) in series. The two parallel branches are connected in series with the load capacitance C as shown in Fig. 4a. The supply voltage for the proposed gates is VDD, which is a slowly varying triangular voltage as shown in Fig. 2a. The experimental work essentially consists of simulating the circuits shown in Figs. 4a and 4b with the circuit parameters as indicated in Section 3.

The simulated values of energy dissipation for the adiabatic NOR and NAND gates corresponding to input strings A = ‘10101010101010101010’ and B = ‘10101010101010101010’ are shown in Table 4 for one cycle of charging and discharging. With a view to comparing this energy dissipation with that of CMOS circuits, the circuits of CMOS NAND and NOR gates are simulated with identical transistors and load capacitance. The supply
voltage for these circuits is 1.8 V. The energy dissipated as measured is given in Table 4, which indicates that in our proposed adiabatic gates, the energy dissipation is only about 50% of that in the CMOS gates.

5 GFCAL adder circuits and JK flip-flop

The block level diagram of our GFCAL half adder is given in Fig. 5a. It consists of one XOR gate and one AND gate. The XOR gate is realised using two NOR gates and one AND gate as shown in Fig. 6. The AND gate is realised by connecting the output of a NAND gate as input to the inverter. The OR gate is realised by connecting the output of a NOR gate as input to the inverter. The load capacitance for the gate in the last stage, which has to drive the next stage, is 30 fF and for all the other gates, the value of the load capacitance is 10 fF (including the input capacitance of the next stage). The supply for all the circuits is a triangular waveform as shown in Fig. 2a. The combination of inputs '00,01,10,11' are given in the form of strings \( A = '01010101' \) and \( B = '00110011' \). The outputs namely the SUM and CARRY are obtained as strings '01100110' and '00010001', respectively. The energy dissipated has been found out through simulation and is shown in Table 5. The simulation of the circuits has been performed for supply frequencies up to 500 MHZ and input data frequencies up to 250 MHZ. To compare this with a CMOS half adder, the CMOS half adder is simulated with identical transistors and a supply of 1.8 V. It has been found that the CMOS half adder takes double the energy consumed by the adiabatic half adder.

Using the half adder as the block, a full adder is simulated according to the circuit shown in Fig. 5b. This consists of two half adders and an OR gate. The performance of this is also evaluated on the same lines as that of the half adder. Typical SUM and CARRY output waveforms for the input strings of \( A = '101010' \) and \( B = '101010' \) and input carry = '101010' are shown in Fig. 7. The CMOS full adder also has been simulated and its performance evaluated. The values of energy dissipated along with the GFCAL full adder are shown in Table 5. From this table, it may be seen that the energy dissipation in the proposed full adder is about 50% of that of a CMOS full adder.

Using a full adder as the block, a 4 bits ripple carry adder is simulated according to the circuit shown in Fig. 5c. This consists of four full adders and the carry output is given as the carry input to the following adder. The measured values of energy dissipated in this circuit and that of the CMOS 4 bits adder with similar circuit parameters are shown in Table 5. From this table, it may be seen that the energy dissipation in the proposed 4 bits ripple carry adder is about 50% compared with that of the CMOS ripple carry adder. The functionality of the circuit is guaranteed by maintaining the supply frequency higher than the frequency of the input data.

The latches are generally realised by connecting two inverters or two NAND/NOR gates in a cross-coupled fashion. The circuit of JK flip-flop is shown in Fig. 8. This circuit consists of four GFCAL NAND gates. The structure of the NAND gate is the same as given in Fig. 4. The inputs are J and K along with the clock signal and \( Q \) and \( Q' \) are the outputs where \( Q' \) is the complement of \( Q \). The supply voltage is \( V_{DD} \), which is a slowly varying triangular voltage as shown in Fig. 2a. The energy

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**Table 4** Comparison of simulated values of energy dissipation for GFCAL NAND and NOR gates and similar CMOS gates for one cycle of charging and discharging at 25 MHZ

<table>
<thead>
<tr>
<th>Name of the circuit</th>
<th>Energy dissipated, J</th>
</tr>
</thead>
<tbody>
<tr>
<td>Proposed GFCAL</td>
<td>CMOS</td>
</tr>
<tr>
<td>NAND gate</td>
<td>( 4.88 \times 10^{-14} )</td>
</tr>
<tr>
<td>NOR gate</td>
<td>( 4.94 \times 10^{-14} )</td>
</tr>
</tbody>
</table>

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**Figure 5** Block level diagrams of

- a GFCAL half adder
- b GFCAL full adder
- c GFCAL 4 bits ripple carry adder
dissipated in the JK flip-flop at an input frequency of 25 MHZ and a supply frequency of 250 MHZ is shown in Table 5. Typical simulation results indicating the transfer of data with respect to time is shown in Fig. 9. From this figure, it may be seen that, when the clock is enabled, the output changes according to the inputs, that is, outputs $Q = '1'$ and $\overline{Q} = '0'$ when $J = '1'$ and $K = '0'$. Similarly, $Q = '0'$ and $\overline{Q} = '1'$ when $J = '0'$ and $K = '1'$. Further, the outputs $Q$ and $\overline{Q}$ are latched to their corresponding values when the clock input is disabled. The functionality of GFCAL hierarchical circuits is ensured by having the supply frequency higher than the frequency of the input data. The energy dissipation in this latch is about 50% of that of the CMOS latch.

Further, the number of transistors in CMOS and our circuit are the same, except that one diode per branch is extra in our circuit. Also, the circuit elements can be designed to make the output logic levels the same as the input logic levels. Thus, the circuits can be easily cascaded. The power saving in these circuits is because of: (i) the supply voltage is a slowly varying voltage, which results in energy saving during charging and discharging; (ii) the energy stored in the load capacitor is pumped back into the supply to realize a transition from logic ‘1’ to logic ‘0’, (iii) there is no short circuit current from the supply to the ground at any time during the transition of logic ‘1’ to logic ‘0’ or logic ‘0’ to logic ‘1’ unlike in the CMOS circuits; and (iv) The diode in the discharge path of the gate prevents the flow of current spikes from the input data into the load capacitor.

### Table 5 Energy dissipation for the proposed GFCAL adder circuits, JK flip-flop and similar CMOS circuits at input frequency of 25 MHZ

<table>
<thead>
<tr>
<th>Name of the circuit</th>
<th>Measured energy, $J$</th>
<th>Logic ‘1’, $V$</th>
<th>Logic ‘0’, $V$</th>
</tr>
</thead>
<tbody>
<tr>
<td>GFCAL half adder</td>
<td>$2.82 \times 10^{-13}$</td>
<td>1.4</td>
<td>0.45</td>
</tr>
<tr>
<td>GFCAL full adder</td>
<td>$7.35 \times 10^{-13}$</td>
<td>1.4</td>
<td>0.45</td>
</tr>
<tr>
<td>GFCAL 4 bits adder</td>
<td>$3.32 \times 10^{-12}$</td>
<td>1.4</td>
<td>0.45</td>
</tr>
<tr>
<td>GFCAL JK flip-flop</td>
<td>$1.28 \times 10^{-13}$</td>
<td>1.4</td>
<td>0.45</td>
</tr>
<tr>
<td>CMOS half adder</td>
<td>$6.21 \times 10^{-13}$</td>
<td>1.78</td>
<td>0.0</td>
</tr>
<tr>
<td>CMOS full adder</td>
<td>$1.67 \times 10^{-12}$</td>
<td>1.78</td>
<td>0.0</td>
</tr>
<tr>
<td>CMOS 4 bits adder</td>
<td>$6.68 \times 10^{-12}$</td>
<td>1.78</td>
<td>0.0</td>
</tr>
<tr>
<td>CMOS JK flip-flop</td>
<td>$2.87 \times 10^{-13}$</td>
<td>1.78</td>
<td>0.0</td>
</tr>
</tbody>
</table>

### 6 Comparison of proposed GFCAL family with other adiabatic logic families

The other adiabatic logic circuits given in [10] are simulated with similar circuit parameters. The length and width of the
transistor are 180 nm and 720 mm, respectively, and the value of load capacitance is 30 fF. This simulation is carried out by keeping the input frequency the same as the supply frequency (25 MHz). A 2N-2N2D inverter uses four-transistors and two-diodes. The capacitor has to be charged first before evaluating the outputs, which may cause unwanted switching activities at the output nodes. A 2N-2P inverter uses four-transistors and a 2N-2N2P inverter uses six-transistors. A PAL inverter uses four-transistors but requires two complementary sinusoidal power clocks in cascaded circuits. A CAL inverter contains eight-transistors and needs a single clock and two additional timing control clocks for correct operation. A True single phase energy recovery logic (TSEL) inverter contains six-transistors and needs a single clock, but it has discharge/charge and evaluation phases, which may cause unnecessary switching activities at nodes in hierarchical circuits. A Quasi-static energy recovery logic (QSERL) inverter contains four-transistors and needs a single clock, but a threshold voltage drop at MOSFETS used as diodes will occur and also the capacitance effect exists at higher frequencies. An ADL inverter contains one-transistor and one diode along with a load capacitor and needs a four-phase clock in cascaded circuits. Since the capacitor has to be pre-charged, unwanted switching activity may occur at the output nodes.

The energy dissipated in the CMOS, GFCAL, ADL, 2N-2N2D, QSERL, 2N-2P, 2N-2N2P and CAL inverters at an input frequency of 25 MHz and a supply frequency of 25 MHz during one cycle of charging and discharging of the load capacitor are $9.12 \times 10^{-14}$, $4.04 \times 10^{-14}$, $3.41 \times 10^{-14}$, $6.64 \times 10^{-14}$, $5.11 \times 10^{-14}$, $5.21 \times 10^{-14}$, $5.26 \times 10^{-14}$ and $5.19 \times 10^{-14}$ J, respectively. At an input
frequency of 125 MHz and a supply frequency of 125 MHz, the energy dissipated in the CMOS, GFCAL, ADL and 2N-2N2D inverters during one cycle of charging and discharging are $9.15 \times 10^{-14}$, $3.84 \times 10^{-14}$, $3.64 \times 10^{-14}$ and $6.51 \times 10^{-14}$ J, respectively. With the above-mentioned transistor parameters, the load capacitor could not be charged and discharged to the required logic levels in the QSERL and the other logic families. However, by increasing the width of the transistor, the load capacitor is charged to appropriate logic levels. When the width of the transistor is increased to 4.0 $\mu$m, the energy dissipated in the GFCAL and QSERL circuits during one cycle of charging and discharging at 125 MHz are $5.48 \times 10^{-14}$ and $6.02 \times 10^{-14}$ J, respectively. Further, a MOSFET diode in the QSERL increases the low logic value to approximately the threshold value of the transistor. This is likely to reduce the noise margins. Also, the capacitive coupling effect of the power supply clock to the output node in some of the cascaded stages may cause unwanted switching activity. As described earlier in GFCAL circuits with a diode, the logic ‘0’ value has been found to be about 0.45 V with a silicon diode, and this can be further reduced if a suitable Schottkey diode is used.

7 Conclusions

This paper reports cascadable adiabatic circuits in which the energy saved has been shown to be more than 50% compared with that of conventional CMOS circuits. Further, it has been argued that this circuit can be used in building hierarchical circuits as the input and output logic levels are the same, just like in the case of conventional digital circuits, and there are no glitches. Further, all the circuits can be operated with a single power supply and there is no need of a complementary input. It has been shown that GFCAL circuits can work well up to 250 MHz using 0.18 micron technology with a reasonable $W/L$ ratio of the transistors.

8 Acknowledgment

The authors would like to thank Prof Govindacharyulu for the discussions that they had with him from time to time.

9 References


