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by

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***Abstract*—In this paper, the optimal transistor sizing of the digital cells has been obtained using Simulated Annealing algorithm and an Artificial Bee Colony algorithm and their results have been compared with nominal results for various nanoscale CMOS digital circuits. The goal is to minimize the leakage power keeping the other performance parameters such as propagation delays and the area in the bound. The simulations are done using HSPICE tool for 45nm and below using Metal gate High k Predictive Technology Model cards. To make sure of the unaffected working of all cells in the automotive applications, the temperature range and supply voltage has been taken between -55^oC to 125^oC and $0.95V$ to $1.05V$ respectively. The Overall reduction in leakage power achieved in the logic cells is up to 70% without any penalty in the critical path delay.**

***Keywords*—Simulated Annealing algorithm (SA), Artificial Bee Colony algorithm (ABC), CMOS, Leakage Power, Propagation Delay**

I. Introduction

Downscaling the technology nodes in CMOS integrated circuits at or below 45nm have fastened the performance of the circuits but at the cost of the power consumption. In ultra-deep sub-micron regime, the leakage power dominates over dynamic power [1] [2]. The major sources of leakage power in CMOS are Junction leakage, Gate induced drain leakage, Gate tunneling leakage and Sub-threshold leakage. Among all these leakages, the sub-threshold leakage is the most dominating [3]. The sub-threshold leakage current can be observed from equation (1).

$$I_{ds} = K(1 - e^{(-V_{ds}/V_T)})e^{(V_{gs}-V_{th0}+\eta V_{ds})/nV_T} \quad (1)$$

where η is drain induced barrier lowering coefficient, K and n are technology functions, V_{ds} and V_{gs} are drain to source and gate to source voltages, V_T is the voltage equivalent to temperature and V_{th0} is the threshold voltage.

Gate oxide leakage currents have been partially limited by the introduction of high-K dielectrics in CMOS technologies [4]. The designer can reduce these leakages keeping other performance specifications in a bound with the two available degrees of freedom ie. the channel length (L) and the channel width (W). At nanoscaled technology nodes, the variation in operating conditions such as temperature and supply voltage can also ruin the system performances [5]. Fig. 1 shows an impact of operating variations on the performances of a full adder cell, it's schematic is displayed in Fig. 6. It can be clearly observed from Fig. 1 that leakage increases exponentially with temperature for all the input vectors. Also, the low to high and high to low delay term from input nodes A, B, C to the carry output Co of 1-bit full adder cell is increased with the reduction in supply voltage. Thus an efficient and robust transistor sizing is required for a circuit to be susceptible to such variations which is the motivation for the author to solve such problems.

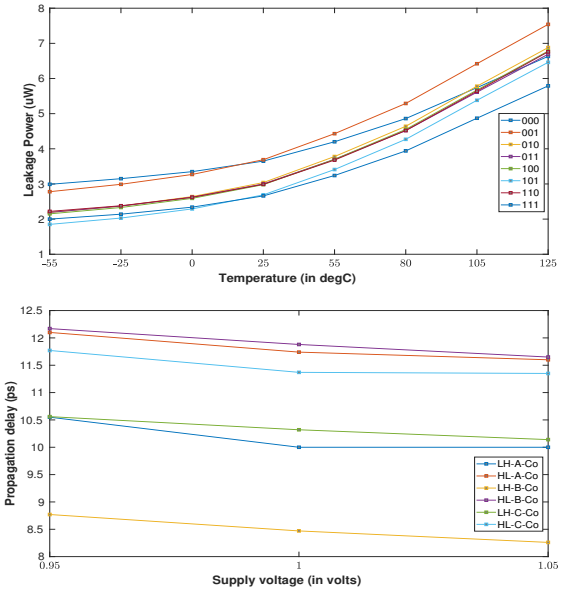


Fig. 1: Impact of operating variations on performances of full adder cell

To wane this issue, Simulated Annealing algorithm (SA) and an Artificial Bee Colony algorithm (ABC) are implemented in this paper to obtain the robust transistor sizing of the various nanoscale digital cells such as 2 input, 3 input CMOS NAND, NOR, AND, OR, XOR and full adder (FA) circuit and then these optimized cells are used in the complex cells such as C17 benchmark, C432 (Interrupt Controller), parity checker, 4 bit multiplier, different 32 bit adder circuit and mitigate the

leakage power, keeping the propagation delays and area in the bound.

In the Annealing process, a metal is first heated until it melts and then it is cooled down slowly so that atoms attain the equilibrium state, as later atoms move less freely with less energy than earlier. The pseudo code of the SA algorithm is displayed in Fig. 2. It begins by generating the random initial solutions. Then random changes are done to the current solution x_c that is proportional to current temperature. Thus the fitness function value obtained at a current solution is compared with that of the new solution x_n obtained. The current solution gets replaced by a new solution if the new solution is better or if the probability function given in equation (2) is higher than a randomly generated number between 0 and 1.

$$p = \frac{1}{1 + e^{\frac{-(E(c,T)-E(n,T)}{T}}} \tag{2}$$

where E(c,T) and E(n,T) are the corresponding energy values of current state (c) and new state (n) respectively.
To avoid premature convergence, the rate of temperature reduction should be slow, as given in equation (3).

$$T_{i+1} = \alpha * T_i \tag{3}$$

where i+1 is the number of iterations and α is the cooling rate ($0 < \alpha < 1$) taken as 0.7 in this paper. In this way, some worse solutions may be accepted at the beginning of the SA, but in the end, only improved ones are allowed. Further information on Multi-Objective SA (MOSA) can be easily found in the survey work in [6].

```
begin
    Initialize(temperature, starting point)
    while cool_iterations <= max_iterations
        temp_iteration = 0
        while temp_iteration <= nrep
            temp_iteration=temp_iteration + 1
            Select a new point in the neighborhod
            Compute the current cost (of this new point)
            δ = current_cost - previous_cost
            if δ < 0 , accept neighbor
            else, accept with the probability given in Eq.2
        end while
        Reduce temperature using Eq.3
    end while
end
```

Fig. 2: Pseudo code for SA algorithm

ABC is a swarm intelligence based optimization algorithm proposed in [7] based on the concept of how artificial bees search for their food. The pseudo code of the algorithm is given in Fig. 3. Here, the bees are of three types; employed bees, onlookers and scouts. The initialization of food sources is given in Eq.4.

$$x_{ij} = x_j^{min} + rand(0,1)\big(x_j^{max} - x_j^{min}\big) \tag{4}$$

where i is number of food sources and j is the number of design parameters. x_j^{min} and x_j^{max} is the minimum and maximum values of parameter j. The employed bees travel to the food sources in the memory and determine the neighbourhood food source given by Eq. 5.

$$v_{ij} = x_{ij} + \phi_{ij}(x_{ij} - x_{kj}) \tag{5}$$

where j and k are randomly chosen parameters and neighbourhoods respectively and ϕ_{ij} is a random number within [-1, 1]. In the algorithm, the one with the highest fitness is selected. After reaching the food source they come back to their hive and dance on this area, the onlooker bee waits on the dance area and makes a decision to choose the food source by evaluating the probability function given by Eq. 6.

$$p_i = fitness_i(x_i) / \sum_{j=1}^{n} fitness_j(x_j) \tag{6}$$

This process will continue until the maximum trial is reached. Scout is a bee that searches food randomly [8] using Eq.4. The working of the ABC algorithm and its performance comparison with other evolutionary and the population based algorithm can be referred from the survey work in [9].

```
begin
    Initialize the food sources =20  trails=100, population of solutions be x_ij and also
    lower bound of parameters.
    Evaluate the population.
    Cycle=1, Maxiter=600.
    for cycle in range(Maxiter) do
        for each employed bee i do
            Choose a food source x_k in the neighborhood of x_i and select jth
            parameter out of total design parameters (D).
            Generate a food source v_i in the neighborhood of x_i and x_k using Eq.5
            Evaluate fitness and select the best between x_i and v_i and increment trails.
        end
        for each onlooker bee i do
            Select a food source x_i based on the probability p_i using Eq.6
            Choose a food source x_k in the neighborhood of x_i
            Generate a food source vi in the neighborhood of x_i and x_k by Eq.5
            Evaluate fitness and select the best between x_i and v_i and increment trails.
        end
        if there exists an abandoned food source or limit has been reached then
            Scout bee determines a new food source by Eq.4
        end
        Memorize the best solution achieved so far.
    end
end
```

Fig. 3: Pseudo code for ABC algorithm

Here, the food can be considered as the minimum value of the solution (leakage power) of the fitness function in the optimization process and the bees as the different transistor sizings, which provide those solutions. In the past years, many comparisons have been done between different evolutionary algorithms and swarm based algorithms. However, no optimal sizing of each transistor has been calculated using the reported algorithms.

The rest of the paper is organized as follows: Section II describes background work; In section III, an implementation of both the algorithms is shown through an example case of CMOS 3-input AND cell. Section IV discusses the obtained results of CMOS 1-bit full adder cell and few multistage/benchmark circuits followed by conclusion in Section V.

II. Background

Various techniques have been reported in the literature to reduce the leakage power in the digital cells. A complete survey on conventional power reduction techniques in standby

as well as in active mode has been done in [10] [11], which includes dual threshold CMOS, Multi-threshold CMOS, Power gating, Input Vector Control (IVC) etc. Many optimization algorithms have been proposed in the past including Genetic Algorithm (GA) [12], Particle swarm optimization (PSO) [13] etc. GA is an effective optimization algorithm which can solve complex non-parametrical problems, multi dimensional, non-continuous and non-differential problems. [12]. But the problem with GA is that it can't provide guaranteed response times and is computationally less efficient, here these response times vary with much larger variance [14]. Swarm intelligence algorithms are the ones which inspired by swarming behaviour of biological population and overcome the time complexity of GA without compromising in quality of solution [13], Particle Swarm Optimisation (PSO) is one of them. Another advantage of swarm algorithms is maintaining of the different population which allows greater diversity and exploration. In the reported work we introduce Artificial Bee Colony (ABC) and Simulated Annealing(SA) implementations on the various digital cells. High robustness, fast convergence and flexibility are the advantages of ABC. In [15] Fatemeh *et al.* presented convex and non-convex modeling of power and delay in VLSI circuits. It also discussed the Weighted Sum and Compromise Programming. A logic-level leakage estimation model is discussed in [16] based on the characterization of voltages at the internal nodes of digital cells. Optimal transistor sizing for multiple logic cells and their yield calculation has been done in [17]. A different parametric yield calculation with transistor sizing approach is proposed in [18] for fully custom circuits.

A comparison of Non-Linear Programming (NLP) and General Geometric Programming (GGP) for low power VLSI circuits have been done in [19].

III. Methodology

In order to calculate the optimal sizing of each transistor in the standard digital cells (SDCs), we have implemented SA and ABC algorithms and compared the performance with the nominal results. The multi-objective optimization generates the Pareto-optimal (PO) solutions, where no other solution exists in the search space that dominates them [20]. The Nominal sizing of the transistors for all the digital cells in this paper have been taken from [17].

TABLE I: Design Parameters Bounds

Technology node	Design Parameter	Lower	Initial	Upper
45nm	L_NMOS (nm)	45	45	50
	L_PMOS (nm)	45	45	50
	W_NMOS (nm)	90	[17]	1000
	W_PMOS (nm)	90	[17]	1000
22nm	L_NMOS (nm)	22	22	25
	L_PMOS (nm)	22	22	25
	W_NMOS (nm)	50	[17]	720
	W_PMOS (nm)	50	[17]	720

The procedure can be easily understood through an example of a CMOS 3 Input AND cell (AND3) shown in Fig.4, which consists of 8 transistors in total, connected in the pull up network and pull down network. SA algorithm and ABC algorithm are applied to optimize the leakage power for all possible eight input combinations 000, ..., 111 simultaneously by varying the design parameters ie. width (W) and length (L) of the transistors in the range given in Table I, with predefined step size in the respective technology nodes. L_NMOS (L_PMOS) and W_NMOS (W_PMOS) are the length and width of the NMOS (PMOS) respectively. The leakage optimization is done keeping all delays arc ('low to high' and 'high to low') in specification bound (critical path delay at initial transistor sizing of respective SDCs). Such circuit sizing procedures are the simulation intensive job, therefore, the circuit sizing scheme runs from 50K to 1Million SPICE simulations (varies on the circuit size, number of performances and operating condition range) in order to fulfil the performance specifications in respective circuits.

The targeted performance results of CMOS AND3 cell obtained through SA and ABC algorithm have been reported in Table II and compared with the respective performance's values at the nominal sizing. In real practice the worst case performances are usually evaluated at model corners to account for the process variation, for instance, delay at slow corner (SS) and leakage at fast corner (FF) are considered. Thus for the corner analysis, we have considered $\pm 5\%$ variation in the threshold voltage (V_t) of the transistors.

At 45nm technology node, the nominal operating conditions (NOC) and worst operating conditions (WOC) are defined as follows:

- In NOC: {temp, V_supply, corner} = {25^oC, $1.0V$, FF / SS}
- In WOC: {temp, V_supply, corner} = {125^oC, $1.05V$, FF} (for leakage computation) and {temp, V_supply, corner} = {-55 to 125^oC, $0.95V$, SS} (for delays computation).

For the CMOS AND3 cell, the WOC conditions for leakage and delays are observed at 125^oC, $1.05V$, FF and 125^oC, $0.95V$, SS respectively. It is depicted in Table II that reduction in the average leakage power at NOC and WOC is achieved up to 25% and 34% with SA and 50% and 55% with ABC respectively. In Table II, the low to high and high to low propagation delays are represented by T_{plh_x} and T_{phl_x}, where x is the input node and the leakage at input vector 'xyz' is given by $Leak\_xyz$. As highlighted in Table. II, the initial delay of the critical path in AND3 cell for NOC and WOC are 14.4 ps and 15.4 ps respectively, which has been taken as a maximum delay bound during the complete optimization procedure. The delays are with in the critical path delay bound of NOC and WOC for both SA and ABC.

Fig. 7 shows the average leakage power obtained for SA and ABC for basic digital circuits at 45nm technology node and Fig. 8 (a) shows their corresponding critical path delay considered as a bound.

To show the technology independent behavior of both the algorithms, we have applied them on other scaled technology nodes also. Table III shows the results of performances

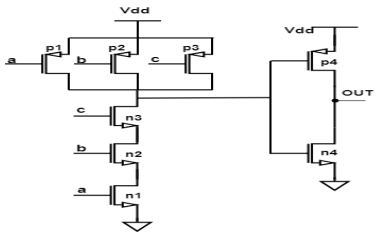


Fig. 4: CMOS 3 input AND cell

obtained for CMOS AND3 cell at 22nm technology node. The range for the design parameters (W and L) for 22nm is reported in Table I.

At this technology node, the NOC and WOC conditions considered are:

- In NOC: {temp, V_supply, corner} = {25^oC, $0.8V$, FF / SS}
- In WOC: {temp, V_supply, corner} = {125^oC, $0.84V$, FF} (for leakage computation) and {temp, V_supply, SS} = {-55 to 125^oC, $0.76V$} (for delays computation).

For CMOS AND3 cell, the worst leakage and delay (WOC) are observed at 125^oC, $0.84V$, FF and 125^oC, $0.76V$, SS respectively. From Table III and Fig. 5, compare to nominal, the average leakage power at NOC and WOC has been reduced up to 22% and 222% with SA and 41.4% and 38.6% with ABC respectively. The critical path delay at the initial sizing is 14.3ps for NOC and 14.7ps for WOC, which have been taken as the maximum bound for all the delays in the optimization process for AND3.

Fig. 5 shows how average leakage power is reduced in AND3 cell with SA and ABC algorithms compared to the nominal leakage power for 45nm and 22nm technology nodes.

TABLE II: Results obtained for CMOS AND3 cell at 45nm technology

Performances	Nominal		SA		ABC	
	NOC	WOC	NOC	WOC	NOC	WOC
Leak_000 (nW)	593	1371	482	951	325	714
Leak_001 (nW)	469	1258	397	878	265	656
Leak_010 (nW)	509	1309	331	765	279	676
Leak_011 (nW)	435	1778	262	921	243	876
Leak_100 (nW)	660	1482	550	1033	337	720
Leak_101 (nW)	612	2016	517	1402	293	803
Leak_110 (nW)	856	2619	529	1132	365	883
Leak_111 (nW)	1142	5938	852	4611	527	2550
T_{plh_a} (ps)	10.2	10.9	14.2	15.2	14.3	15.3
T_{phl_a} (ps)	**14.4**	**15.4**	14.1	15.0	14.4	15.4
T_{plh_b} (ps)	10.1	10.8	14.0	15.1	14.4	15.4
T_{phl_b} (ps)	12.7	13.5	10.9	11.5	14.1	15.0
T_{plh_c} (ps)	9.5	10.1	13.8	14.8	14.1	15.1
T_{phl_c} (ps)	10.7	11.3	11.2	11.8	12.5	13.2
$(W/L)_{p1}$	360/45		294/45		205/47	
$(W/L)_{p2}$	360/45		487/48		180/47	
$(W/L)_{p3}$	360/45		286/45		180/47	
$(W/L)_{n1}$	540/45		440/48		247/45	
$(W/L)_{n2}$	540/45		386/45		201/47	
$(W/L)_{n3}$	540/45		251/48		180/48	
$(W/L)_{p4}$	360/45		259/48		296/48	
$(W/L)_{n4}$	180/45		160/47		180/45	

TABLE III: Results obtained for CMOS AND3 cell at 22nm technology

Performances	Nominal		SA		ABC	
	NOC	WOC	NOC	WOC	NOC	WOC
Leak_000 (nW)	322	750	280	667	239	618
Leak_001 (nW)	268	714	243	649	210	598
Leak_010 (nW)	300	771	260	681	217	613
Leak_011 (nW)	287	1284	265	1098	209	829
Leak_100 (nW)	524	1014	428	842	312	705
Leak_101 (nW)	548	1625	430	1156	304	865
Leak_110 (nW)	815	2030	563	1299	378	860
Leak_111 (nW)	940	1380	620	998	475	791
T_{plh_a} (ps)	13.0	13.3	14.0	14.3	14.3	14.4
T_{phl_a} (ps)	**14.3**	**14.7**	11.9	12.1	14.26	14.5
T_{plh_b} (ps)	12.9	13.2	14.0	14.4	14.3	14.5
T_{phl_b} (ps)	13.1	13.4	12.8	13.0	14.3	14.6
T_{plh_c} (ps)	12.2	12.5	13.6	14.0	14.0	14.2
T_{phl_c} (ps)	11.6	11.7	11.9	12.0	14.3	14.5
$(W/L)_{p1}$	176/22		198/22		130/22	
$(W/L)_{p2}$	176/22		136/22		115/22	
$(W/L)_{p3}$	176/22		134/22		101/22	
$(W/L)_{n1}$	264/22		218/22		123/22	
$(W/L)_{n2}$	264/22		146/22		96/22	
$(W/L)_{n3}$	264/22		123/22		88/24	
$(W/L)_{p4}$	176/22		168/22		283/23	
$(W/L)_{n4}$	88/22		86/22		95/23	

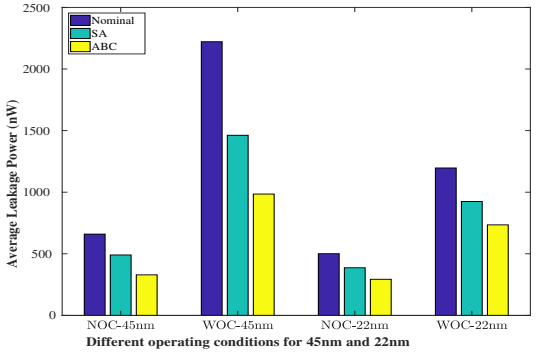


Fig. 5: Average leakage power obtained for AND3 cell at different operating conditions and technology nodes used.

IV. Results & Discussion

Table IV shows the performances obtained for the CMOS NAND3 digital cells at 45nm technology using reported algorithms. The worst leakage and delay (WOC) are observed at 125^oC, $1.05V$, FF and 125^oC, 0.95, SS respectively. The initial critical path delay for NOC and WOC is maintained as upper limit correspondingly while minimizing the leakage power of the circuit. The average leakage reduction in NOC and WOC with SA are 37% and 41% and with ABC are 49% and 52% compared to those of the initial respectively.

The methodology is also applied on 32nm in addition to 45nm and 22nm MGK using PTM model cards on various CMOS SDCs of different fan-in. We are not reporting the sizing, individual performance analysis and schematic of all the circuits due to space limitations. However, we are reporting the results of a full adder, one of the pivotal building block in processor design. The targeted CMOS full adder design is shown in Fig. 6 which consists of 28 transistors in mirror

TABLE IV: Results obtained for CMOS NAND3 cell at 45nm technology

Performances	Initial		SA		ABC	
	NOC	WOC	NOC	WOC	NOC	WOC
$Leak\_000$ (nW)	384	666	297	495	264	436
$Leak\_001$ (nW)	260	552	201	382	188	351
$Leak\_010$ (nW)	300	603	223	413	192	354
$Leak\_011$ (nW)	225	1060	149	575	136	520
$Leak\_100$ (nW)	451	776	292	491	256	419
$Leak\_101$ (nW)	402	1290	227	659	200	518
$Leak\_110$ (nW)	646	1890	346	785	281	623
$Leak\_111$ (nW)	970	5290	533	3324	463	2700
T_{plh_a} (ps)	**10.9**	**11.8**	9.34	10.1	10.8	11.8
T_{phl_a} (ps)	6.10	6.15	10.5	10.5	10.8	11.1
T_{plh_b} (ps)	9.46	10.3	10.6	11.5	10.9	11.8
T_{phl_b} (ps)	6.08	6.13	10.3	10.4	10.9	11.1
T_{plh_c} (ps)	7.74	8.45	8.43	9.18	10.8	11.9
T_{phl_c} (ps)	5.49	5.53	10.0	10.2	10.8	10.4
$(W/L)_{p1}$	360/45		308/45		274/46	
$(W/L)_{p2}$	360/45		268/47		261/47	
$(W/L)_{p3}$	360/45		306/47		227/47	
$(W/L)_{n1}$	540/45		273/45		246/45	
$(W/L)_{n2}$	540/45		314/45		251/47	
$(W/L)_{n3}$	540/45		177/48		218/47	

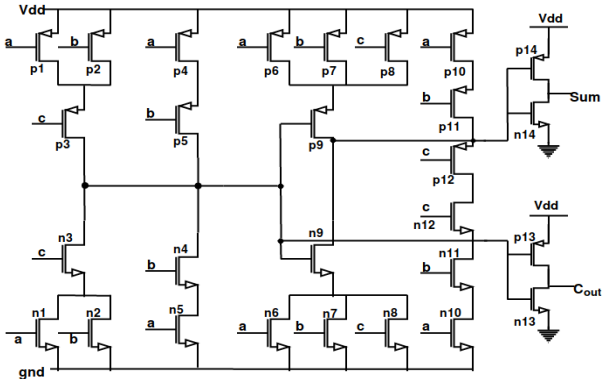


Fig. 6: CMOS 28T Full Adder Cell

TABLE V: Results obtained for CMOS 28T 1-bit Full Adder cell at 45nm technology

Performances	Nominal		SA		ABC	
	NOC	WOC	NOC	WOC	NOC	WOC
$Leak\_000$ (µW)	3.98	9.61	2.16	5.05	1.69	3.96
$Leak\_001$ (µW)	4.13	13.31	2.16	5.69	1.61	4.31
$Leak\_010$ (µW)	3.47	12.03	1.99	5.57	1.47	4.42
$Leak\_011$ (µW)	3.42	13.29	2.02	6.59	1.74	6.99
$Leak\_100$ (µW)	3.41	11.93	1.85	5.75	1.54	4.51
$Leak\_101$ (µW)	3.11	12.62	1.67	6.84	1.49	6.30
$Leak\_110$ (µW)	3.41	12.91	1.75	6.28	1.53	6.33
$Leak\_111$ (µW)	3.01	13.35	1.72	6.27	1.39	4.95
$T_{plh\_a\_Cout}$ (ps)	13.2	13.8	15.1	15.9	14.1	15.4
$T_{phl\_a\_Cout}$ (ps)	14.8	15.9	15.08	16.1	14.7	16.0
$T_{plh\_b\_Cout}$ (ps)	11.5	12.1	12.5	13.5	14.2	15.6
$T_{phl\_b\_Cout}$ (ps)	**15.1**	**16.1**	14.9	16.0	14.8	15.8
$T_{plh\_c\_Cout}$ (ps)	13.3	13.6	14.3	14.9	14.5	15.5
$T_{phl\_c\_Cout}$ (ps)	14.9	15.7	15.07	16.1	14.7	15.9
$(W/L)_{p1}$	720/45		496/48		498/45	
$(W/L)_{p2}$	720/45		354/47		448/46	
$(W/L)_{p3}$	720/45		486/47		527/46	
$(W/L)_{n1}$	360/45		267/45		210/45	
$(W/L)_{n2}$	360/45		320/47		180/45	
$(W/L)_{n3}$	360/45		333/46		303/45	
$(W/L)_{p4}$	720/45		611/45		529/46	
$(W/L)_{p5}$	720/45		430/48		496/45	
$(W/L)_{n4}$	360/45		334/46		329/47	
$(W/L)_{n5}$	360/45		224/46		234/45	
$(W/L)_{p6}$	720/45		683/47		180/46	
$(W/L)_{p7}$	720/45		192/48		180/45	
$(W/L)_{p8}$	720/45		334/47		180/45	
$(W/L)_{p9}$	720/45		185/45		180/45	
$(W/L)_{n6}$	360/45		239/46		180/45	
$(W/L)_{n7}$	360/45		188/48		180/45	
$(W/L)_{n8}$	360/45		357/47		180/45	
$(W/L)_{n9}$	360/45		275/47		180/45	
$(W/L)_{p10}$	1080/45		412/47		180/46	
$(W/L)_{p11}$	1080/45		259/45		180/45	
$(W/L)_{p12}$	1080/45		307/46		180/46	
$(W/L)_{n10}$	540/45		374/48		180/45	
$(W/L)_{n11}$	540/45		193/46		180/47	
$(W/L)_{n12}$	540/45		333/45		180/47	
$(W/L)_{p13}$	720/45		376/45		562/47	
$(W/L)_{n13}$	360/45		350/46		352/45	
$(W/L)_{p14}$	720/45		242/45		180/45	
$(W/L)_{n14}$	360/45		214/47		180/46	

fashion. The obtained sizing of basic SDCs are applied to various benchmark and multistage complex circuits in order to validate the leakage reduction efficiency of the proposed methodology while improving/keeping delays and area in the bound. Table V shows the performances obtained in 1-bit Full adder cell in the case of NOC and WOC for SA and ABC algorithm, and their results are compared with nominal values. Even here, the NOC is maintained at 25^oC, $1.0V$, FF / SS and the worst leakage and delay (WOC) are observed at 125^oC, $1.05V$, FF and 125^oC, $0.95V$, SS respectively. As shown in Fig. 7 for a full adder, the average leakage power at NOC and WOC has been reduced up to 40% and 45% with SA and up to 55% and 60% with ABC respectively compared to initial. While, the initial delay of the critical path for carry output of NOC and WOC are 15.1ps and 16.1ps respectively, which is taken as a limit for final critical path delay.

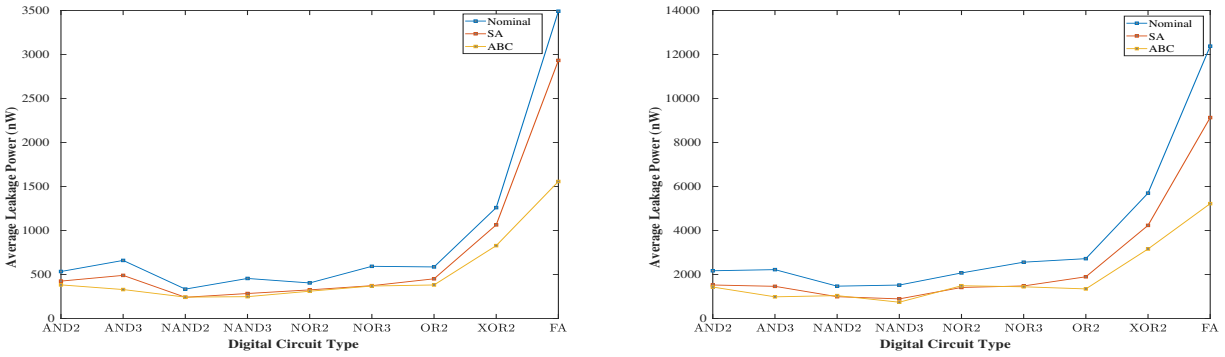
Fig. 7 shows the average leakage power obtained for various logic cells at 45nm technology node for the mentioned approaches and compared the results with the nominal results keeping the delays in the initial critical path delay bound as shown in Fig. 8 a).

Table VI shows total average power obtained (including both static power and dynamic power) for different basic digital circuits for 2fF capacitive load. Their circuit diagrams and nominal sizing can be referred from [17].

The optimal transistor sizing obtained from SA and ABC for basic digital circuits can be used to implement different standard benchmark circuits. Table VII shows the average leakage power obtained at different operating conditions for C17 cell, Parity checker, C432 (Interrupt Controller), 4-bit Multiplier, 32-bit ripple carry adder, 32-bit carry select adder, 32-bit carry save adder while keeping the delays in the limit of the critical path of the initial.

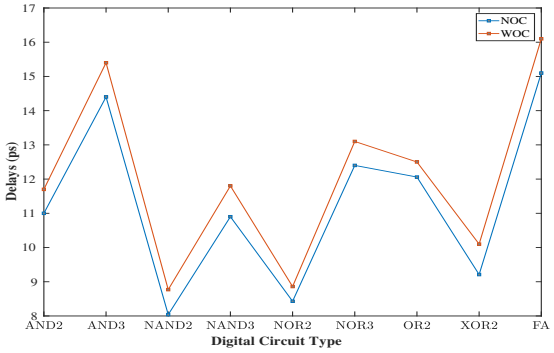
V. CONCLUSION

In this paper, we have implemented Simulated Annealing algorithm and an Artificial Bee Colony algorithm to obtain the operating variation invariant transistor sizing for optimal



(a) (b)

Fig. 7: Average leakage power obtained in CMOS basic digital circuits at 45nm technology a) at NOC b) at WOC.



(a)

Fig. 8: Initial critical path delay considered for various SDCs at 45nm technology

TABLE VI: Total average power obtained for SDCs at 45nm technology

Sr. No.	Digital Circuit Type	Total Average Power (μW)					
		Nominal		SA		ABC	
		NOC	WOC	NOC	WOC	NOC	WOC
1	$AND2$	0.93	1.36	0.87	1.1	0.74	1.49
2	$AND3$	1.95	2.43	1.60	1.87	1.31	1.48
3	$NAND2$	0.86	1.14	0.33	0.62	0.73	0.93
4	$NAND3$	1.53	1.86	1.07	1.24	1.02	1.14
5	$NOR2$	1.04	0.81	0.87	0.70	0.69	0.86
6	$NOR3$	2.10	2.37	1.42	1.58	1.4	1.56
7	$OR2$	1.35	2.32	1.09	1.39	1.03	1.508
8	$XOR2$	1.60	2.49	1.4	2.0	1.14	1.55
9	28-T *Full Adder*	13.4	14.6	8.15	8.44	7.37	7.75

leakage power, propagation delay and area in various digital circuits and compared the obtained results with nominal results. It can be stated from the results that in most of the circuits ABC performs better than the SA algorithm in terms of power and delay. The transistor sizing has calculated for each circuit is invariant of temperature for automotive applications and $\pm$ 5% variation in supply voltage with process corners analysis. The average leakage reduction is obtained up to 70% in SDCs. The rise and fall time both for the clock and data input are taken as 10ps. The setup and hold time are taken as 1ns and 3ns respectively. The run time of the ABC algorithm is the product of number of design parameter, max. iteration and food sources. However, the computation time to fully optimize one circuit is approximately 0.5 hour for SA algorithm and 1.5 hours for ABC algorithm based approach considering 400 iterations on 32 GB RAM, 12 core machine.

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TABLE VII: Results obtained for complex cells at $45\mathrm{nm}$ technology

Sr. No.	Digital Circuit Type	Average Leakage Power (μW)					
		Nominal		SA		ABC	
		NOC	WOC	NOC	WOC	NOC	WOC
1	$C17$	2.12	8.33	1.40	4.74	1.56	5.91
2	$Parity\ Checker$	9.45	39.25	8.00	27.56	8.0	27
3	$C432\ (Interrupt\ Controller)$	11.6	39.5	8.63	28.24	8.84	28.86
4	$4\ Bit\ Multiplier$	52.89	153.8	9.6	30.6	25.6	75.85
5	$32\ Bit\ Ripple\ Carry\ Adder$	106.0	372.0	59.07	184.48	49	165.0
6	$32\ Bit\ Carry\ Select\ Adder$	227.08	765.02	127.0	389	106.4	349
7	$32\ Bit\ Carry\ Skip\ Adder$	378.03	892.01	283.6	596.7	260	530

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