67 ppm/°C, 66nA PVT Invariant Curvature Compensated Current Reference for Ultra-Low Power Applications

by

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Abstract—This work presents a highly accurate current reference of 66nA for ultra-low power applications. A very low figure-of-merit (FOM) of 1.3501ppm/°C² is achieved on consuming a minimal quiescent current of 199.37nA. To cancel out process variations, the current subtraction technique is employed and a β-multiplier is used to compensate for mobility (μ) and threshold voltage (Vth). In addition, curvature compensation technique backed by PTAT and CTAT current cancellation is adopted to attain a lower temperature coefficient (TC). Hence, an imperceptible variation of accuracy with temperature and supply variations across all process corners is attained. An adopted trimming scheme further minimizes the overall process spread to ±1.515% without compromising on accuracy. Accordingly, a TC of 67.04ppm/°C over a wide temperature range of -50°C to 100°C is obtained. Furthermore, 1.413%/V line sensitivity (LS) in the supply range of 1.38V to 3V is observed. Low power consumption of 275.13nW@1.38V facilitates its use in high-performance low power applications.

Index Terms—FOM, curvature compensation, Line Sensitivity, Proportional to Absolute Temperature (PTAT), Complementary to Absolute Temperature (CTAT), ZTC

I. INTRODUCTION

Thriving demand for energy harvesters [1], biomedical devices like Cochlear implants [2], gastric electrical stimulator [3], etc. led to a greater requirement for circuits engrossing less quiescent current. To support these applications there is a necessity to design ultra-low power analog and mixed-signal modules like Op-Amps, Oscillators, ADC’s, DAC’s, etc. Current reference is one of the critical blocks involved in these above mentioned modules. Designing high accurate (PVT invariant) current reference (nA range) with low power consumption in scaled CMOS technologies has been a major challenge for analog designers.

In the literature survey, distinct techniques have been proposed [4]–[11] to enhance the performance across PVT variations. Ueno et al. [5] has reduced the active area (0.015mm²) to a great extent by biasing MOSFET as a resistor in β—multiplier. But the power consumption (1μW) and TC (520ppm/°C) of the generated 96nA @ 1.8V reference is high. Hirose et al. [6] used the technique of current subtraction where power consumption (88.53nW) is remarkably low with an outstanding supply regulation (0.046%/V). But the achieved TC (1190ppm/°C) in -20°C to 80°C range is considerably high. Bendali et al. [7] used the concept of biasing the MOSFET at ZTC to generate 144.3μA. With a low supply voltage (1V), a TC of 185ppm/°C in the limited temperature range (0-100°C) is achieved. Osipov et al. [8] used the first-order temperature compensation technique to generate 1.05μA. A satisfactory TC of 143ppm/°C is attained but the minimum voltage of 2.2V is required. Lee et al. [9] and Jain et al. [10] used the concept of dividing PTAT voltage with resistor of PTAT temperature dependency to boost the accuracy but these designs involved op-amp as an integral part. Mohamed et al. [11] proposed a current reference based on curvature compensation scheme which minimized the TC to 40ppm/°C. But the power consumed is 820.8nW and the supply range (1.2V to 2V) is limited.

In the light of this background, a curvature compensated current reference for wide temperature and supply range is proposed. As shown in Fig. 1, PTAT current is added to the CTAT current resulting in \( I_{REF_1} \). Similarly, a non-linear CTAT current is added to PTAT current resulting in \( I_{REF_2} \). Finally, \( I_{REF_1} \) and \( I_{REF_2} \) are summed up to get curvature compensated current reference \( I_{REF} \) as shown in Fig. 1. This brief is organized as follows. Section II explains the proposed architecture, Section III summarizes the obtained results and Section IV draws the conclusions.

II. PROPOSED ARCHITECTURE

The proposed architecture has three considerable segments as shown in Fig. 2.

A. PTAT current generator \( (I_{PTAT}) \)

To generate PTAT current, a β-multiplier circuit is used as shown in Fig. 2 \( (I_{PTAT}-GENERATOR) \). Current through the

Fig. 1. Block diagram of the proposed architecture

MOSFET
poly resistor \( R_1 \) is given by:
\[
\frac{V_{GS7} - V_{GS8}}{R_1} = I_1
\]  

(1)

current through the MOSFET in sub-threshold region for \( V_{DS} > 0.1V \) [5], [12] is given by:
\[
I_D = \mu C_{ox} \frac{W}{L} (\eta - 1)V_T^2 \exp\left(\frac{V_{GS} - V_{th}}{\eta V_T}\right)
\]  

(2)

where \( \mu \) is the carrier mobility, \( C_{ox} \) is the gate-oxide capacitance, \( \eta \) is the sub-threshold slope factor, \( V_T = \frac{K_BT}{q} \) is the thermal voltage, \( K_B \) is the Boltzmann constant, \( q \) is the elementary charge, \( T \) is the temperature and \( V_{th} \) is the threshold voltage of a MOSFET.

Hence from (1) and (2), current \( I_1 \) is given as:
\[
I_1 = \frac{\eta V_T \ln \frac{K_8}{K_7}}{R_1} + \delta V_{th} \frac{K_8}{R_1}
\]  

(3)

where \( \delta V_{th} = V_{th7} - V_{th8} \). \( K_7 \) and \( K_8 \) are the sizes of \( M_7 \) and \( M_8 \) respectively. In (3), the second term (\( \delta V_{th}/R_1 \)) is negligible in comparison with first term. Hence,
\[
I_1 = \frac{\eta V_T \ln \frac{K_8}{K_7}}{R_1}
\]  

(4)

(4) illustrates that \( I_1 \) is independent of process parameters (\( \mu \), \( V_{th} \)) and supply voltage. The poly resistance can be modelled as \( R_1 = R_0(1 + \alpha \cdot T) \) [13], [9] where, \( \alpha \) is a process independent temperature coefficient. Differentiating (4) with respect to temperature results in:
\[
\frac{1}{I_1} \frac{\partial I_1}{\partial T} = TC_{11} = \frac{1}{V_T} \frac{\partial V_T}{\partial T} - \frac{1}{R_1} \frac{\partial R_1}{\partial T}
\]  

(5)

(4) and (5) concludes that the current \( I_1 \) can be adjusted to have PTAT behaviour (as shown in Fig. 3) by appropriate sizing of \( M_7 \) and \( M_8 \). Hence, \( I_1 = I_{PTAT} \).

B. CTAT current generator-1 (\( I_{CTAT1} \))

To generate CTAT current, the circuit shown in Fig. 2 (\( I_{CTAT1-GENERATOR} \)) is proposed. MOSFET’s \( M_9 \) - \( M_{16} \) forms the Widlar current source which contributes for supply independence. \( M_{17} \) is a diode connected MOSFET whose \( V_{SG} \) appears across \( R_2 \) (as \( V_{GS18} \approx V_{GS16} \)). Therefore,
\[
I_2 = \frac{V_{SG17}}{R_2}
\]  

(6)

The CTAT behaviour of \( V_{SG} \) in a diode connected MOSFET is well explained in [14]. It is modelled as \( V_{SG} = V_{SG_o} - K_{VSG}T \) where, \( V_{SG_o} \) is the \( V_{SG} \) at \( 0K \) and \( K_{VSG} \) is the temperature coefficient of \( V_{SG} \). Differentiating (6) with respect to temperature results in:
\[
\frac{1}{I_2} \frac{\partial I_2}{\partial T} = \frac{1}{V_{SG17}} \frac{\partial V_{SG17}}{\partial T} - \frac{1}{R_2} \frac{\partial R_2}{\partial T}
\]  

(7)

\[
TC_{12} = TC_{V_{SG17}} + (-1 \cdot TC_{R_2})
\]  

(8)

From (8), it is evident that generated current exhibits negative temperature coefficient (Fig. 3a). Hence, \( I_2 = I_{CTAT1} \).

C. CTAT current generator-2 (\( I_{CTAT2} \))

To achieve the curvature compensation as shown in Fig. 1, another CTAT current with non-linear temperature dependency is generated. MOSFET’s \( M_{21} \) - \( M_{25} \) (Fig. 2) forming a \( \beta \)-multiplier contributes for supply independence. \( M_{27} \) is biased with a supply independent node voltage \( V_{GS7} \) \((\leq V_{th27})\) to ensure its operation in sub-threshold region. Besides, \( M_{18} \) and \( M_{19} \) are biased with \( V_{GS20} + V_{GS22} \) and \( V_{GS20} \) respectively such that \( I_{18} > I_{19} \). Hence, these MOSFET’s (\( M_{18} \) and \( M_{19} \)) perform a critical role in current subtraction thereby eliminating process variations whose mathematical analysis is presented below. Subtracted current \( I_3 = I_{18} - I_{19} \) is given by,
\[
I_3 = \beta(K_{18} \exp \frac{V_{GS18} - V_{th18}}{V_T} - K_{19} \exp \frac{V_{GS19} - V_{th19}}{V_T})
\]  

(9)

where, \( \beta = \mu C_{ox} \). \( K_{18} \) and \( K_{19} \) are the sizes of \( M_{18} \) and \( M_{19} \) respectively. Temperature dependency of mobility as given in [5] shows that \( \mu \propto T^{-m} \) where, \( m \) is mobility temperature exponent. Hence, the current \( I_3 \propto \beta \) has non-linear negative temperature dependency (\( \cdot \); \( I_3 = I_{CTAT2} \)). To validate the process independency, (9) is differentiated with respect to process and resultant is equated to zero [15].
\[
\frac{\partial I_3}{\partial P} = 0
\]  

(10)

On simplification, the resultant can be approximated as,
\[
\frac{K_{19}}{K_{18}} = \exp \left( \frac{V_{GS18} - V_{GS19}}{V_T} \right)
\]  

(11)

Therefore, \( M_{19} \) and \( M_{18} \) are biased such that \( V_{GS18} - V_{GS19} = 0.5V_T \) and their sizes are chosen accordingly (\( K_a = 1.68K_0 \)) thereby resulting in cancellation of process variation. Moreover, any supply variations across \( M_{18} \) and \( M_{19} \) are eliminated due to current subtraction.
### Table I : PERFORMANCE SUMMARY AND COMPARISONS WITH RELATED WORKS

<table>
<thead>
<tr>
<th>PARAMETERS</th>
<th>THIS WORK</th>
<th>[11]</th>
<th>[16]</th>
<th>[17]</th>
<th>[6]</th>
<th>[5]</th>
<th>[8]</th>
</tr>
</thead>
<tbody>
<tr>
<td>Technology (µm)</td>
<td>0.18</td>
<td>0.18</td>
<td>0.18</td>
<td>0.35</td>
<td>0.35</td>
<td>0.35</td>
<td>0.35</td>
</tr>
<tr>
<td>Supply Range (V)</td>
<td>1.38 - 3</td>
<td>1.2 - 2</td>
<td>1.2 - 1.8</td>
<td>1.9 - 3.6</td>
<td>1.3 - 3</td>
<td>1.8 - 3</td>
<td>1.2 - 3.6</td>
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<tr>
<td>$I_{REF}$ (nA)</td>
<td>66</td>
<td>142.5</td>
<td>92.3</td>
<td>16000</td>
<td>9.95</td>
<td>96</td>
<td>1050</td>
</tr>
<tr>
<td>TC(±ppm/°C)</td>
<td>67.04</td>
<td>40</td>
<td>179.9</td>
<td>105</td>
<td>1190</td>
<td>520</td>
<td>143</td>
</tr>
<tr>
<td>Temperature Range(°C)</td>
<td>-50 - 100</td>
<td>-40 - 85</td>
<td>-40 - 85</td>
<td>0 - 110</td>
<td>-20 - 80</td>
<td>0 - 80</td>
<td>-40 - 120</td>
</tr>
<tr>
<td>Line Sensitivity (%/V)</td>
<td>1.413</td>
<td>1.45</td>
<td>7.5</td>
<td>4</td>
<td>0.046</td>
<td>0.2</td>
<td>2.73</td>
</tr>
<tr>
<td>$I_{total} / I_{REF}$</td>
<td>3.0209</td>
<td>4.8</td>
<td>4</td>
<td>2</td>
<td>6.844</td>
<td>3.47</td>
<td>1.9523</td>
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<tr>
<td>FOM(±ppm/°C²)</td>
<td>1.3501</td>
<td>1.54</td>
<td>6.59</td>
<td>1.9</td>
<td>81.44</td>
<td>22.56</td>
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<td>Area(mm²)</td>
<td>0.098</td>
<td>0.02</td>
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<td>0.065</td>
<td>N/A</td>
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<td>0.057</td>
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<td>Power(nW)</td>
<td>275.13</td>
<td>820</td>
<td>670</td>
<td>60800</td>
<td>88</td>
<td>1000</td>
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<td>Trimming</td>
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<td>No</td>
<td>No</td>
<td>Yes</td>
<td>No</td>
<td>No</td>
<td>No</td>
</tr>
</tbody>
</table>

#### D. Temperature compensation

Two current references $I_{REF1} (= I_{PTAT} + I_{CTAT1})$ and $I_{REF2} (= k.I_{PTAT} + I_{CTAT2})$ with opposite curvatures are generated as shown in Fig. 3a and 3b which are in turn summed up proportionately to get curvature compensated current reference. From (4) and (6), $I_{REF1}$ can be written as:

$$I_{REF1} = \frac{1}{R_1} \eta V_T \ln \frac{K_8}{K_7} + \frac{V_{GS12}}{R_2}$$  \hspace{1cm} (12)

In (12), the sizes of $M_7$ and $M_8$ are adjusted accordingly thereby resulting in $I_{REF1}$ with the curvature as shown in Fig. 3a. From (4) and (9), $I_{REF2}$ can be written as:

$$I_{REF2} = \frac{k}{R_1} \eta V_T \ln \frac{K_8}{K_7} + \beta(K_{18exp} \frac{V_{GS18} - V_{th18}}{\eta V_T} - K_{19exp} \frac{V_{GS19} - V_{th19}}{\eta V_T})$$  \hspace{1cm} (13)

Hence, $I_{REF2}$ with the curvature as shown in Fig. 3b is obtained by appropriate sizing of $M_7$, $M_8$, $M_{18}$ and $M_{19}$. Finally, $\alpha_1 I_{REF1}$ and $\alpha_2 I_{REF2}$ are added up to result in curvature compensated $I_{REF}$ (Fig. 4) where $k$, $\alpha_1$ and $\alpha_2$ are scaling factors.

In order to avoid the zero current operating condition of self-biased circuits, a start-up circuit shown in Fig. 2 is employed [18]. Though the slope of $I_{REF}$ is unvaried due to the introduced compensation, the amplitude of $I_{REF}$ still varies in different process corners as shown in Fig. 6a. Hence, a trimming circuit is additionally employed (Fig. 2) to reduce this process spread.

#### III. RESULTS AND DISCUSSION

The proposed circuit has been implemented in TSMC 180nm technology. The temperature sensitivity (over the range of -50°C to 100°C at 1.38V supply) and LS (over the range of 1.38V to 3V at 27°C) of $I_{REF}$ in TT corner are plotted as shown in Fig. 4 and 5 respectively. Hence, a TC of 67.04 ppm/°C and LS of 1.413%/V is noted. Furthermore, the TC and LS of $I_{REF}$ is monitored across all possible skewed corners (Fig. 6a and 6b). An average TC and LS of 66ppm/°C and 1.52%/V is observed respectively.

A 5-bit trimming circuit [19] is employed to minimize the process spread. The value of $I_{REF}$ with all possible trim codes is plotted in different process corners as shown on Fig. 7. From this, we can infer that the trim codes for $I_{REF} = 66nA$ are 01010, 11001, 00000 and 10011 in SS, FS, SF and FF respectively. The trimming circuit is inactive for trim codes 01111 and 10000 (Fig. 2). The temperature sensitivity of $I_{REF}$ in TT, SS, FF, SF and FS after trimming is plotted as shown in Fig. 8.

To test the robustness of the design with PVT variations, monte-carlo simulation on $I_{REF}$ at 27°C and TC at a supply of 1.38V is done for 1000 samples (Fig. 9a and 9b). The mean ($\mu$) of 66.25nA and 65.92ppm/°C and a standard deviation ($\sigma$) of 2.65nA and 11.3ppm/°C are obtained for $I_{REF}$ and TC respectively. Also, FOM is examined for the total assessment of proposed design in terms of TC, temperature range, $I_{REF}$ and $I_q$ [11].

$$FOM(\frac{\text{ppm}}{\text{°C}^2}) = \frac{TC(\text{ppm}/\text{°C}) \cdot I_q(nA)}{Temp.\text{Range}(\text{°C}) \cdot I_{REF}(nA)}$$  \hspace{1cm} (14)

The monte-carlo simulation is performed on FOM for 1000 samples where $\mu$ and $\sigma$ are observed to be 1.816ppm/°C² and 0.432ppm/°C² respectively.

The variation of $I_{REF}$ with load resistance is shown in Fig. 10b from which it is evident that the proposed $I_{REF}$ can
support the loads up to 22MΩ. Besides, a noise analysis is also presented for different process corners as shown in Fig. 11. An optimized layout is done for the proposed design as shown in Fig. 12. The design occupies an active area of 0.098mm$^2$. Additionally, Table I presents the comparison of the proposed architecture with recent endeavors. It is evident that the proposed work provides a relatively stable current for wide temperature and supply voltage range across all the process corners.

IV. CONCLUSION

A highly stable ultra-low power CMOS current reference using curvature compensation scheme is proposed. It is able to achieve relatively low temperature coefficient with unaltered slope in all possible skewed corners. The design can work for a minimum supply voltage of 1.38V which makes it attractive for low voltage applications. Moreover, it operates over a wide range of temperature and supply voltage. From the obtained specifications, it can be concluded that the proposed design is reliable for high precision low-power applications.
REFERENCES


