A 47nW, 0.7-3.6V wide Supply Range, Resistor Based Temperature Sensor for IoT Applications

by

Zia Abbas, Saikiran Lade, Arpan Jain, Ashfakh Ali

Report No: IIIT/TR/2019/-1

Centre for VLSI and Embeded Systems Technology
International Institute of Information Technology
Hyderabad - 500 032, INDIA
October 2019

A 47nW, 0.7-3.6V wide Supply Range, Resistor Based Temperature Sensor for IoT Applications

Ashfakh Ali, Sai Kiran, Arpan Jain, Zia Abbas
International Institute of Information Technology, Hyderabad (IIIT-H), India
(huluvallay.md, arpan.jain)@research.iiit.ac.in, saikiran.lade@students.iiit.ac.in, zia.abbas@iiit.ac.in

***Abstract*—A sub $1-V$, ultra low power temperature sensor has been implemented in TSMC $180\ nm$. The architecture is digital friendly since it creates a pulse width modulated wave instead of voltage. It uses proportional to absolute temperature(PTAT) characteristics of resistance to generate PTAT delay. Temperature to delay conversion depends only on passive elements, thereby making the circuit insensitive to supply variations. Line sensitivity of $0.23\ ^{\circ}C/V$ is achieved for a wide supply range of $0.7-3.6\ V$. A non linearity error of less than $0.8\ ^{\circ}C$ is measured for $-55\ to\ 125\ ^{\circ}C$ using linear fit curve. This occupies an area of $0.82\ mm^2$ and consumes a power of $47\ nW$ at $0.8\ V$ supply.**

***Index Terms*—Energy harvester, LDO, PSRR, BJT, ADC**

I. Introduction

Sensors have radically changed the way we understand and interact with our world, in real time. Rapid improvements in technology, including miniaturization and advanced microprocessor integration without detracting from performance, make the range of sensor applications almost endless. Many critical applications today including IoT demand these sensors to work with either energy from energy harvesters or energy from miniaturized batteries. Circuits powered by energy harvesters are desired to work at lower supply voltages as well as at low power, while circuits powered by miniaturized batteries are desired to work at low power as well as wide supply range. Temperature sensors, being integral sensing modalities must be designed to satisfy these demands. Temperature is preferably converted to digital code for easy further processing.

Survey of relevant past works reveal that temperature to digital conversion can be done in many ways. Temperature is transduced to 1) voltage followed by ADC to convert the voltage to digital code 2) delay followed by Time to digital conversion 3) frequency followed by frequency to digital conversion. Traditional temperature sensors belong to Type 1. They use the difference between base emitter voltage of BJT to generate a highly linear temperature to voltage conversion [1]–[4]. High precision delta sigma modulators are usually chosen in these architectures for voltage to digital conversion. Although state-of-the-art accuracies have been reported using this architecture, they cannot work with lower supply voltage and consume power in the order of micro watt [5]. To alleviate these issues, type 1 non BJT solutions are explored in [6]–[8]. Although these work with low supply voltages they also consume power in the order of microwatt.

978-1-7281-3915-9/19/$31.00 ©2019 IEEE

Low supply voltage and low power realization of time to digital converters and frequency to digital converters make type 2 and 3 more favourable for ultra low power circuits [9]–[12]. However to make the complete temperature to digital conversion in ultra low power, it is equally important to realize 'temperature to delay' or 'temperature to frequency' conversion in ultra low power. Ultra low power temperature to delay converters are reported in [10], [13], while temperature to frequency converters are reported in [14], [15]. One of the common design challenges of these designs is that they work for a very low supply range. For instance [13] consumes an ultra low power of 75nW but it works for a low supply range of 0.6V-1.2V. Further increasing supply degrades the linearity of these sensors as well as shoots up the power consumption. These circuits need an LDO when they are powered by miniaturized batteries [16]. This further adds its own power consumption. Moreover none of these reported ultra low power designs work in the military temperature range.

A 47nW temperature to delay converter is presented for wide supply range of 0.7-3.6V and temperature range of $-55\ to\ 125\ ^{\circ}C$. The working of the sensor at lower supply voltage and ultra low power consumption makes it suitable to work with energy harvesters, while wide supply range and higher PSRR makes it suitable for working with miniaturized batteries preluding the need of LDO. Rest of the paper is organized as follows. Section 2 provides the working of the proposed architecture. Section 3 provides the simulation results. Finally, Section 4 draws the conclusion.

II. Proposed Architecture

The proposed architecture has 3 major components. 1) Temperature to current converter 2) Ramp generator 3) Always on comparator. The complete block diagram of architecture is shown in Fig.1.

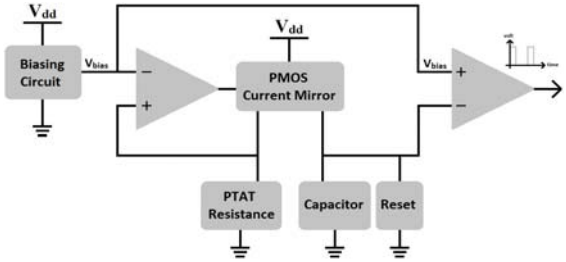

Fig. 1. Block diagram of proposed architecture

Negative feedback of the op amp forces the current through the resistance to be $\frac{V_{bias}}{R_{PTAT}}$. This current is mirrored into the capacitor using a high impedance current mirror. This current is used to charge a periodically-reset capacitor to generate a ramp of slope $\frac{V_{bias}}{R_{PTAT} \cdot C}$. This ramp is compared with the same V_{bias} to generate pulse width modulated wave. On-time of the pulse width modulated wave (T_{on}) is calculated below.

$$\frac{V_{bias}}{R_{PTAT} \cdot C} \cdot T_{on} = V_{bias} \tag{1}$$

cancelling V_{bias} on both sides.

$$T_{on} = R_{PTAT} \cdot C. \tag{2}$$

'rnlpoly' resistance is considered for linear PTAT behaviour. Temperature variation of 'rnlpoly' is shown in Fig. 2 , while Fig. 3 shows the non linearity error of resistance Vs temperature using linear fit curve in MATLAB. A maximum non linearity error of less than 0.2% across process corners makes it appropriate to neglect higher order temperature dependencies on resistance. Modelling of this resistance has been done as in [17].

$$R_{PTAT} = R_0(1 + \alpha \cdot T) \tag{3}$$

where R_0 is a process dependent term while α is a process independent temperature coefficient. α is plotted with temperature across process corners in Fig. 4. The invariance of α with process corners can be noticed from Fig. 4. This has been well explained in [18]. 'crtmom' capacitance is chosen. 'crtmom' capacitance Vs temperature plot is shown in Fig. 5. A maximum absolute deviation of capacitance (from constant value) of less than 0.3% makes it appropriate to take capacitance as constant with temperature. so,

$$T_{on} = R_0 C(1 + \alpha \cdot T) \tag{4}$$

$$T_{on} = T_0 \cdot (1 + \alpha \cdot T) \tag{5}$$

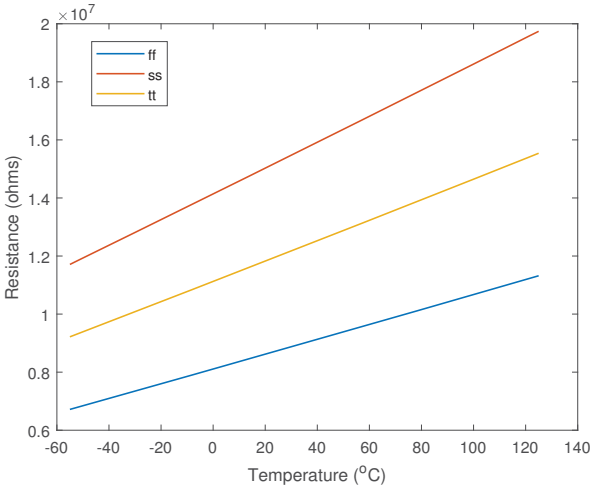

Fig. 2. Resistance Linearity

where $T_0 = R_0 \cdot C$ is a process dependent term, while α is a process independent term as explained earlier. It can be deduced from eq.4 that T_{on} varies linearly with temperature. However, It should be noted that this linear relation of T_{on}

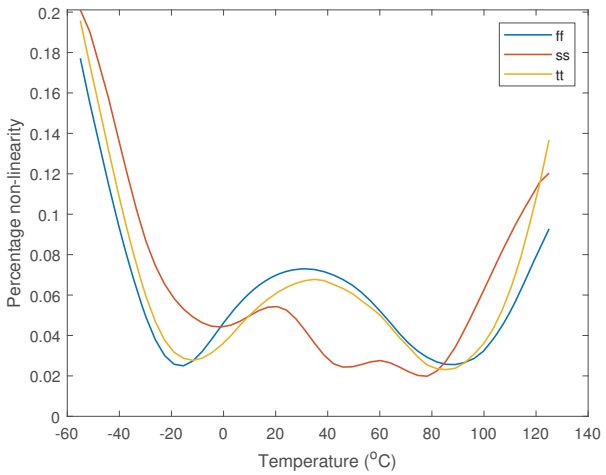

Fig. 3. Percentage Non linearity error of Resistance

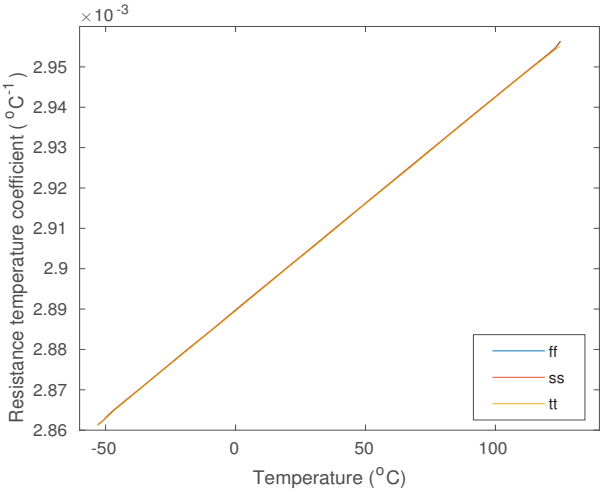

Fig. 4. Resistance temperature coefficient(α) Vs Temperature

with temperature in eq.5 is deduced by assuming V_{bias} to be constant for one reset time period, so that V_{bias} gets cancelled as in eq.1. Now, V_{bias} must be designed to satisfy this assumption. To get the design constraints on V_{bias} consider the expression below.

$$V_{bias} = V_0 + f(P, V, T). \tag{6}$$

V_0 is a PVT invariant voltage. $f(P, V, T)$ is a function that outputs a voltage depending on process (P), supply voltage (V) and temperature (T). Since supply and temperature may change with time, V_{bias} is a function of time. Design constraints on V_{bias} are gradually derived in the following four cases.

Case 1 : $f(P, V, T)$ is a constant voltage, independent of P,V and T. This implies that V_{bias} is constant as a function of time, thereby cancelling V_{bias} as in eq.1 to get delay (T_{on}) independent of V_{bias}.

Case 2 : $f(P, V, T)$ depends only on process and is independent of supply voltage and temperature. Although V_{bias} depends on process, this is a constant with time. So, V_{bias} gets again cancelled as in eq.1. This implies that V_{bias} need

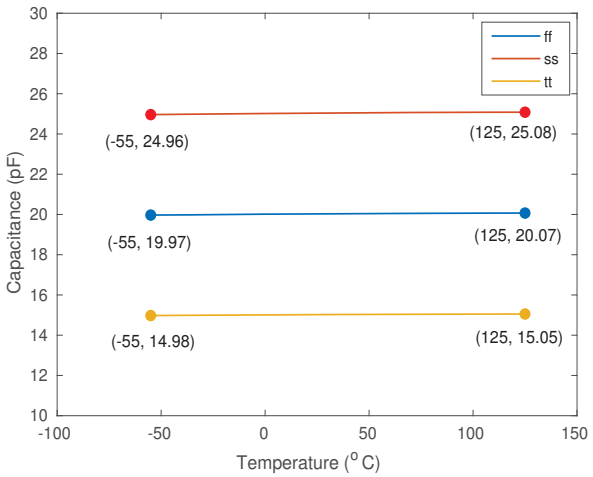

Fig. 5. Capacitance Vs Temperature

not process invariant or no process trimming is required for V_{bias}.

Case 3 : $f(P,V,T)$ depends on process and temperature and is independent of supply voltage. Since chosen frequency of the system (i.e reset frequency of capacitor= 1KHz) is roughly two-three orders (100-1000) of magnitude of actual frequency of temperature variation as evident from [19]. So, temperature can be assumed to be constant for one reset time period (1/f). So, V_{bias} again gets cancelled as in eq.1. This implies that V_{bias} need not be constant with temperature.

Case 4 : $f(P,V,T)$ depends on process, temperature and supply. Lower frequency variations in supply gets cancelled as with the case with temperature (like in case-3) . However, since supply variations can be in any frequency, so V_{bias} needs to be supply independent for getting cancelled as in eq.1

These four cases imply that V_{bias} can be sensitive to process and temperature variations. This architecture requires merely supply independent voltage biasing. Our discussion has so far ignored the non-idealities like charge injection and leakage through the reset switch. Since we have chosen capacitance of 20pf, the effect of charge injection is negligible. Leakage current increases with temperature, so making current in current mirror (Fig.1) to be much greater than leakage current even at high temperatures becomes a design constraint. If V_{bias} is designed as supply independent voltage that decrease with temperature, As R_{PTAT} also increases with temperature the current (V_{bias}/R_{PTAT}) in current mirror (Fig.1) decreases a lot with temperature. It may so happen that this current may become comparable with leakage current at higher temperatures. So, it is desired to design V_{bias} as supply independent voltage that increases with temperature, so that current in PMOS current mirror (Fig.1) may still remain to be much greater than leakage current even at higher temperatures.

Discussion so far, has imposed few design constraints on V_{bias} generating circuitry. They are summarised here 1) Implementation in Ultra low power 2) High PSRR for wide supply range 3) Usability of the circuit even at lower supply voltages 4)V_{bias} should increase with temperature. Taking these design constraints into account, V_{bias} generating circuit is designed as in Fig. 7. To understand this consider Fig. 6 above.

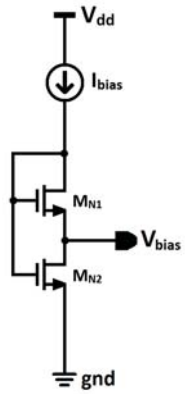

Fig. 6. supply independent voltage generator

Circuit shown in Fig. 6 is first introduced in [20]. The expression for V_{out} is derived in [20], [21] and is included below for clarity.

$$V_{out} = \frac{KT}{q} \ln \left[\frac{(W_1/L_1)}{(W_2/L_2)} \right] \tag{7}$$

This expression is derived in [20] by assuming both Mosfets M_{N1} and M_{N2} to be in sub-threshold region. so, this circuit works with few nA of biasing current. It is evident from the above expression that V_{out} is independent of I_{bias} and increases with temperature. However in reality, V_{out} has slight dependence on I_{bias}. This is because of the fact that [20] ignores the DIBL coefficient in current voltage characteristics as in [22]. I_{bias} generated from conventional current biasing circuits overshoots with supply. This makes V_{bias} sensitive to supply variations. To avoid this I_{bias} is taken from supply independent current generator. This prevents overshooting of current as well as enhances supply rejection of V_{bias}. The complete schematic of voltage bias generating circuit is shown in Fig.7 and its working is explained below.

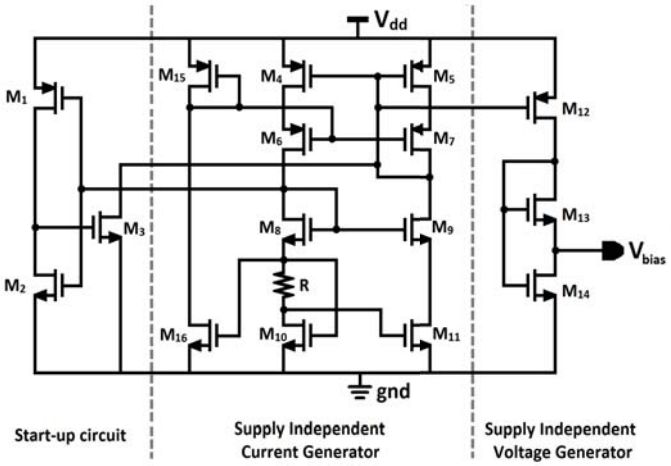

Fig. 7. Voltage Bias Generating Circuit

Mosfets M_1, M_2 and M_3 comprise the start up circuit. Mosfets M_{10}, M_{11} and Resistance(R) comprise the basic supply

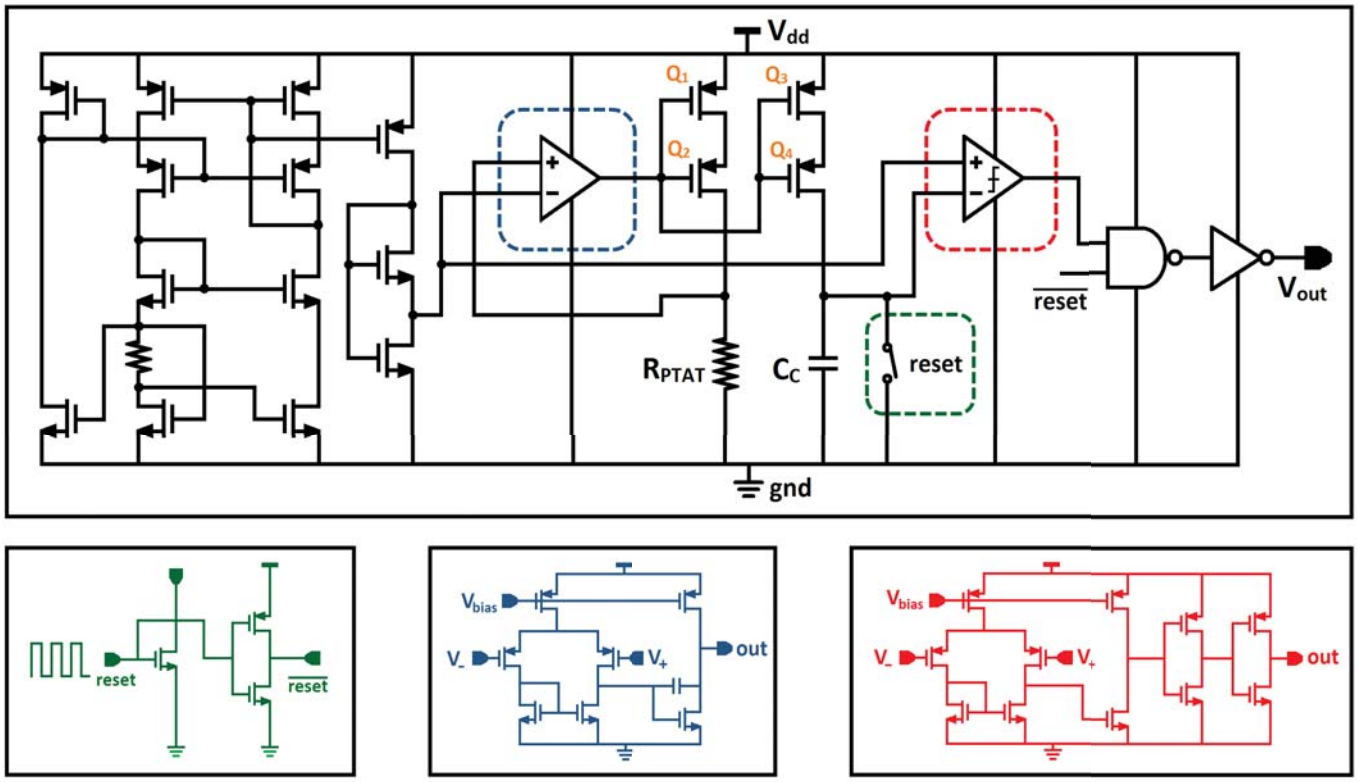

Fig. 8. Complete Schematic of Temperature Sensor.

independent current generating circuitry as in [23]. cascoding is further used to enhance the supply insensitivity of current. Regular cascoding consumes higher voltage headroom thereby inhibiting the circuit to work at lower supply voltage. so, high swing cascode is formed by Mosfets ($M_4 - M_7$). Mosfets M_{15}, M_{16} are used to bias the cascoded transistors. This supply independent current is mirrored into M_{12} to generate supply independent voltage bias. An output capacitor of 1pf is placed to V_{bias} to introduce a pole at lower frequencies for transfer characteristics of V_{bias} with respect to supply. This pole inhibits the degradation of PSRR at higher frequencies.

The complete schematic of the proposed architecture is shown in Fig.8. To avoid complexity, start up circuit is avoided in Fig.8. The 3-dB bandwidth of the op amp is chosen to be greater than the system frequency (i.e Reset frequency of the capacitor = 1KHz) for proper operation. Considering the power bandwidth trade-off, this op amp is designed for 75dB gain and 12nW power consumption using 2 stage miller compensated op amp. This gain is enough for tracking V_{bias} from voltage bias generating circuitry across R_{PTAT}.

A self cascode current mirror (formed by Q_{1-4}) as in [24] is chosen to mirror the current through the resistance into the capacitor. It offers high output impedance as well as consume lower voltage headroom enabling the circuit operation for sub 1V power supply. This current charges a periodically reset capacitor to generate a linear ramp. This ramp is compared with the same V_{bias} using an always on comparator. Conventional 2 stage uncompensated op amp is used as always on comparator. Supply and temperature dependence of the comparator delays are reduced by careful transistor sizing.

III. Results and Discussion

The proposed design is implemented in TSMC 180nm technology. As discussed in section 2, A supply insensitive I_{bias} is required to prevent overshooting of I_{bias} as well as enhance supply insensitivity of V_{bias}. For the targetted supply range of 0.7-3.6V, I_{bias} has a maximum variation of 2nA as evident from Fig. 9. This I_{bias} insensitivity to supply is enough to make V_{bias} supply independent. PSRR of V_{bias} is plotted in Fig. 10 at 0.8V and 3.6V supply voltages respectively.

A best case PSRR of -66.3dB and worst case of -49dB is shown in Fig. 9 at 0.8V and 3.6V supply respectively. An output capacitor of 1pf placed at output of V_{bias} prevents degradation of PSRR at higher frequencies by introducing a pole. This can be noticed from Fig. 10. V_{bias} is plotted with supply in Fig. 11. V_{bias} line sensitivity of 0.063%/V is achieved for wide supply range of 0.7-3.6V.

Current through R_{PTAT} is made almost constant by adjusting temperature coefficient of V_{bias} to be equal to temperature coefficient of R_{PTAT} (as in [18]), so that this current(around 10nA) is much higher than the leakage current through the switch(around 50pA) even at higher temperatures. Time(T_{on}) is plotted with temperature in Fig. 12. Non linearity error of T_{on} is plotted with temperature across process corners in Fig. 13. A maximum non linearity error of 0.2% (0.8 $^{\circ}C$) can be seen from Fig. 13.

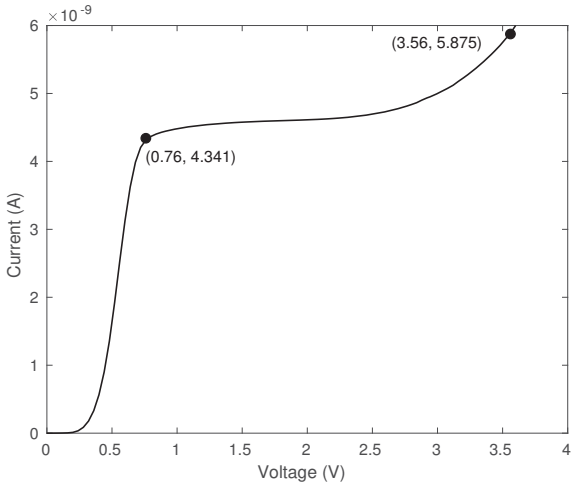

Fig. 9. Line sensitivity of current generator

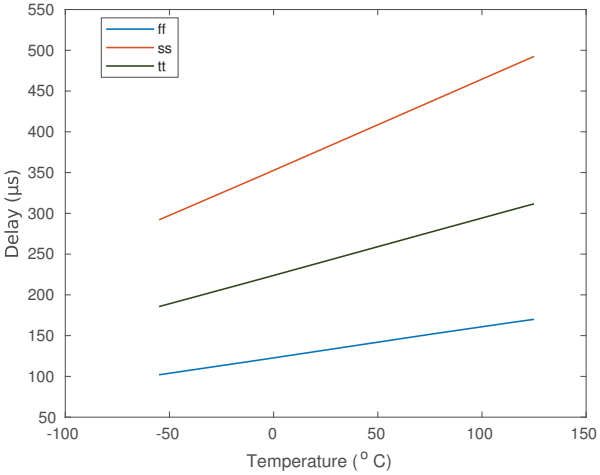

Fig. 12. T_{on} Vs Temp

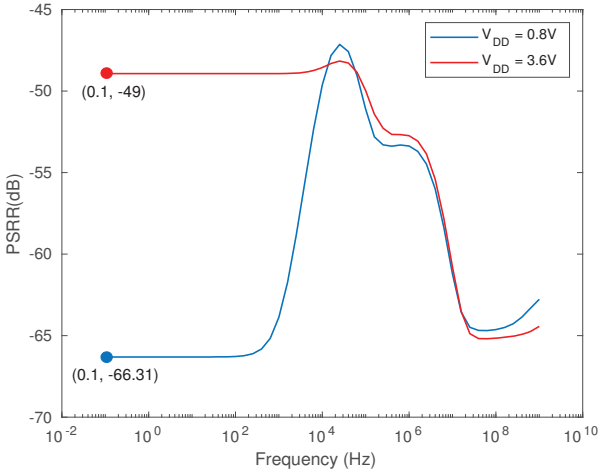

Fig. 10. PSRR of V_{bias}

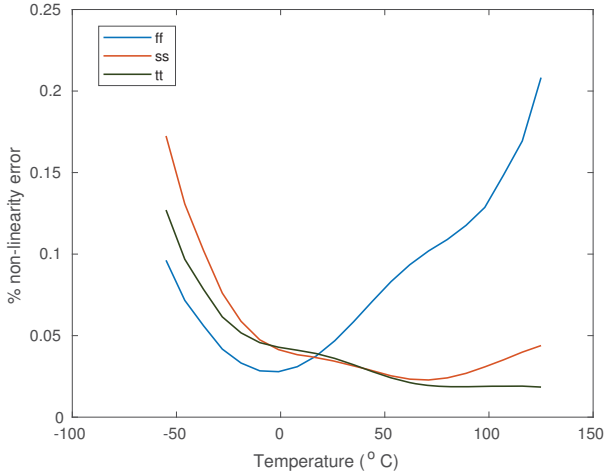

Fig. 13. % nonlinearity of T_{on} Vs Temp

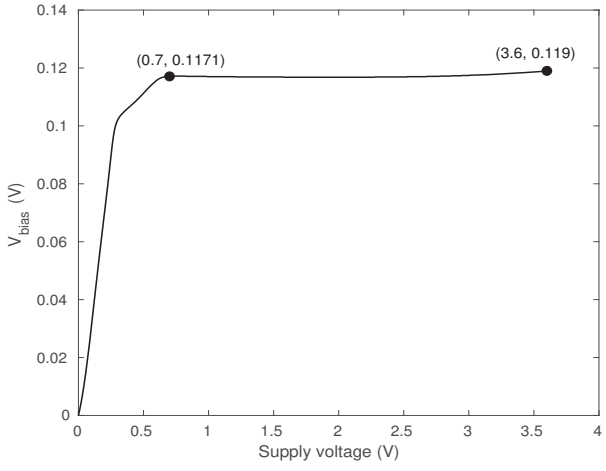

Fig. 11. Line sensitivity of V_{bias}

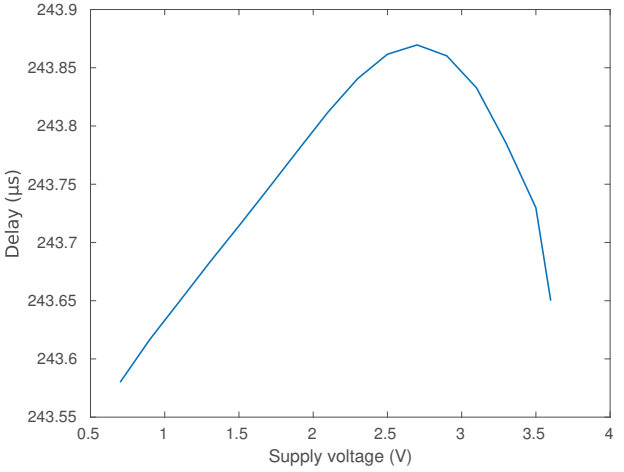

Fig. 14. T_{on} Vs supply variation of 0.7-3.6V

Sensor	This work	[6]	[10]	[13]	[14]
Technology (nm)	180	65	180	180	180
Temp. Range (°C)	-55 to 125	-45 to 85	0 to 100	0 to 100	0 to 100
Supply Range (V)	0.7-3.6	0.6-1.2	-	0.55-1	-
Inaccuracy (°C)	±0.4	±4	+1/-0.8	+0.62/-1.33	+1.5/-1.4
Calibration	1	1	2	2	2
Supply Sensitivity (°C/V)	0.23	0.28	-	1.67	-
Area (mm^2)	0.82	0.044	0.0324	0.45	0.09
Power (nW)	47	47200	405	75	71

Fig. 15. Comparison with other temperature sensors

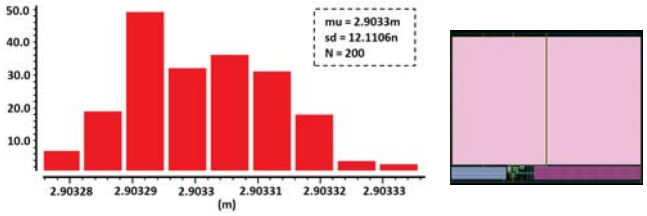

Fig. 16. Montecarlo of Temperature coefficient of T_{on} ($/\ ^\circ C$) and layout of the temperature sensor

Delay vs supply voltage is plotted in Fig. 14 for a wide supply range of 0.7-3.6V. A line sensitivity of $0.23\ ^\circ C/V$ is achieved for a wide supply range of $0.7-3.6\ V$. A comparison table of recently published low power designs is given above. From Fig. 12 it can be seen that T_{on} varies with process since resistance and capacitance change with process, but temperature coefficient of T_{on} which is same as temperature coefficient of resistance(α) is independent of process. so, one point calibration is enough. Montecarlo simulations of temperature coefficient of T_{on} is plotted in Fig. 16.a for 200 samples. A standard deviation of 12.11n for a mean of 2.9m confirms the invariablity to temperature coefficient of T_{on} with process and mismatch variations. Fig. 16.b shows the layout of temperature sensor. The proposed sensor occupies an area of $0.82mm^2$.

IV. CONCLUSION

An ultra low power temperature sensor is proposed. This sensor outputs a PTAT delay using PTAT characteristics of resistance. This delay depends only on passive elements thereby making the sensor immune to supply variations. A supply independent bias circuit is proposed to enhance the supply insensitivity of the sensor as well as prevent overshooting of the circuit even at higher supply voltages.

REFERENCES

[1] M. A. Pertijs, A. Niederkorn, X. Ma, B. McKillop, A. Bakker, and J. H. Huijsing, "A cmos temperature sensor with a 3σ inaccuracy of $\pm 0.5^\circ$C $from\ -50^\circ$C $to\ 120^\circ$C," *IEEE Journal of solid-state circuits*, vol. 40, no. 2, pp. 454–461, 2005.

[2] K. Souri and K. A. Makinwa, "A $0.12mm^2$ $7.4\mu w$ micropower temperature sensor with an inaccuracy of $\pm 0.2^\circ c(3\sigma)$ from $30^\circ to 125^\circ c$," *IEEE Journal of Solid-State Circuits*, vol. 46, no. 7, pp. 1693–1700, 2011.

[3] B. Yousefzadeh, S. H. Shalmany, and K. A. Makinwa, "Bjt-based temperature-to-digital converter with $\pm 60\ mk\ (3\sigma)$ inaccuracy from -70°C $to\ 125^\circ$C in 160 nm cmos," *IEEE Journal of Solid-State Circuits*, vol. 52, no. 4, pp. 1044–1052, 2017.

[4] K. Souri, Y. Chae, and K. A. Makinwa, "A cmos temperature sensor with a voltage-calibrated inaccuracy of $\pm 0.15^\circ$C $(3\sigma)\ from\ -55^\circ$C $to\ 125^\circ$C," *IEEE journal of solid-state circuits*, vol. 48, no. 1, pp. 292–301, 2013.

[5] T. Anand, K. A. Makinwa, and P. K. Hanumolu, "A vco based highly digital temperature sensor with $0.034\ ^\circ\mathrm{C}/m\mathrm{V}$ supply sensitivity," *IEEE Journal of Solid-State Circuits*, vol. 51, no. 11, pp. 2651–2663, 2016.

[6] H. Park and J. Kim, "A 0.8-v resistor-based temperature sensor in 65-nm cmos with supply sensitivity of 0.28 c/v," *IEEE Journal of Solid-State Circuits*, vol. 53, no. 3, pp. 906–912, 2018.

[7] S. K. Maddikatla and S. Jandhyala, "An accurate all cmos temperature sensor for iot applications," in *2016 IEEE Computer Society Annual Symposium on VLSI (ISVLSI)*, pp. 349–354, IEEE, 2016.

[8] Y. Jeong and F. Ayazi, "Process compensated cmos temperature sensor for microprocessor application," in *2012 IEEE International Symposium on Circuits and Systems*, pp. 3118–3121, IEEE, 2012.

[9] M. K. Law, A. Bermak, and H. C. Luong, "A sub-μW embedded cmos temperature sensor for rfid food monitoring application," *IEEE Journal of Solid-State Circuits*, vol. 45, no. 6, pp. 1246–1255, 2010.

[10] M. K. Law and A. Bermak, "A 405-nw cmos temperature sensor based on linear mos operation," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 56, no. 12, pp. 891–895, 2009.

[11] A. Vaz, A. Ubarretxena, I. Zalbide, D. Pardo, H. Solar, A. Garcia-Alonso, and R. Berenguer, "Full passive uhf tag with a temperature sensor suitable for human body temperature monitoring," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 57, no. 2, pp. 95–99, 2010.

[12] Z. Shenghua and W. Nanjian, "A novel ultra low power temperature sensor for uhf rfid tag chip," in *2007 IEEE Asian Solid-State Circuits Conference*, pp. 464–467, IEEE, 2007.

[13] X. Wang, P.-H. P. Wang, Y. Cao, and P. P. Mercier, "A 0.6 v 75nw all-cmos temperature sensor with 1.67 m c/mv supply sensitivity," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 64, no. 9, pp. 2274–2283, 2017.

[14] S. Jeong, Z. Foo, Y. Lee, J.-Y. Sim, D. Blaauw, and D. Sylvester, "A fully-integrated 71 nw cmos temperature sensor for low power wireless sensor nodes," *IEEE Journal of Solid-State Circuits*, vol. 49, no. 8, pp. 1682–1693, 2014.

[15] D. A. Kamakshi, A. Shrivastava, and B. H. Calhoun, "A 23 nw cmos ultra-low power temperature sensor operational from 0.2 v," in *2015 IEEE SOI-3D-Subthreshold Microelectronics Technology Unified Conference (S3S)*, pp. 1–3, IEEE, 2015.

[16] L. Lu, S. T. Block, D. E. Duarte, and C. Li, "A 0.45-v mosfets-based temperature sensor front-end in 90 nm cmos with a noncalibrated $\pm 3.5^\circ$C 3σ relative inaccuracy from -55°C $to\ 125^\circ$C," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 60, no. 11, pp. 771–775, 2013.

[17] R. Baker, "Cmos circuit design, layout, and simulation, revised 2nd ed," *IEEE Press Series on Microelectronic Systems*, 2004.

[18] J. Lee and S. Cho, "A 1.4-μw 24.9-ppm/ c current reference with process-insensitive temperature compensation in 0.18-μm cmos," *IEEE Journal of Solid-State Circuits*, vol. 47, no. 10, pp. 2527–2533, 2012.

[19] A. Miqdad, K. Kadir, and S. F. Ahmed, "Development of data acquisition system for temperature and humidity monitoring scheme," in *2017 IEEE 4th International Conference on Smart Instrumentation, Measurement and Application (ICSIMA)*, pp. 1–4, IEEE, 2017.

[20] E. A. Vittoz and O. Neyroud, "A low-voltage cmos bandgap reference," *IEEE Journal of Solid-State Circuits*, vol. 14, no. 3, pp. 573–579, 1979.

[21] P. C. Crepaldi, T. C. Pimenta, R. L. Moreno, L. B. Zoccal, and L. H. de Carvalho Ferreira, "Low-voltage, low-power vt independent voltage reference for bio-implants," *Microelectronics Journal*, vol. 43, no. 1, pp. 43–49, 2012.

[22] Y. Tsividis and C. McAndrew, *Operation and Modeling of the MOS Transistor*, vol. 2. Oxford university press Oxford, 1999.

[23] B. Razavi, *Design of analog CMOS integrated circuits*. MC Graw Hill, 2005.

[24] I. Fujimori, "Low voltage self cascode current mirror," Oct. 12 1999. US Patent 5,966,005.